

TetraMAX ATPG

Automatic Test Pattern Generation

Overview

TetraMAX® ATPG automatically generates high quality manufacturing test vectors. TetraMAX is the only ATPG solution optimized for a wide range of test methodologies that's integrated with Synopsys' DFT MAX, the leading test synthesis tool. The unparalleled ease-of-use and high performance provided by TetraMAX allows RTL designers to quickly create efficient, compact tests for even the most complex designs.

Key Benefits

- Increases product quality with generated test vectors for high defect detection
- Reduces testing costs through the use of advanced vector compaction techniques
- Increases designer productivity by leveraging integration with Synopsys DFT MAX
- Creates tests for complex and multi-million gate designs

Key Features

- Extremely high capacity and performance
- Integrated graphical user interface
- Integrated simulation waveform viewer
- Integrated context-sensitive online help
- Comprehensive scan design rule checking
- Utilizes existing Verilog simulation libraries
- DSMTTest option supports testing for timing-related deep submicron defects
- IddQTest option available for quiescent test validation
- Integrated fault simulator for functional vectors
- Distributed Processing runs across multiple processors
- Yield Diagnostics with automatic defect isolation

Testing Complex ASICs

With TetraMAX ATPG, designers can generate high quality manufacturing test vectors without compromising on high-performance design techniques. While such techniques may impede older generation ATPG tools, TetraMAX is able to obtain coverage on the resulting complex logic.

TetraMAX supports internal three-state busses including implementations with pull-ups, pull-downs and charge storage. Similar to three-state busses, bi-directional I/O pads are also supported. To ensure ATE (automatic-test-equipment) requirements are met, TetraMAX provides a number of options to generate contention-free vectors for three-state logic.

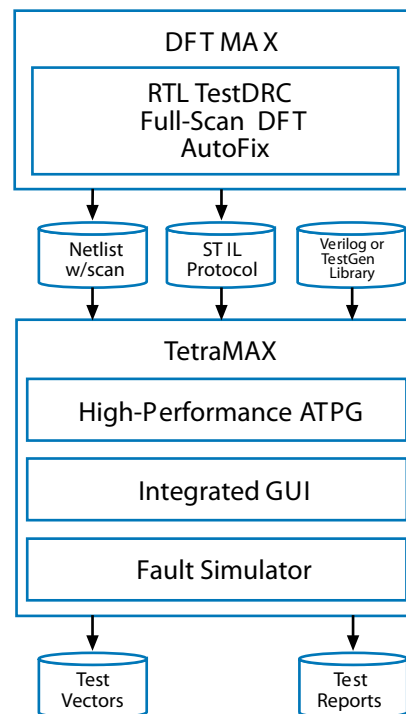


Figure 1: Integrated Test Flow Using TetraMax ATPG.

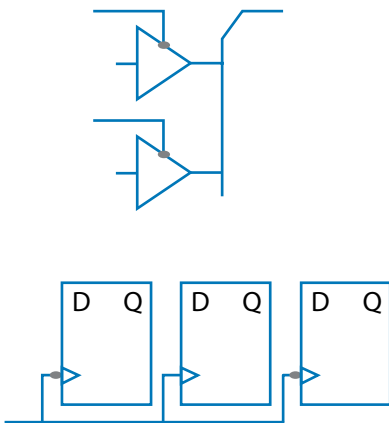


Figure 2: Testing Complex ASICs.

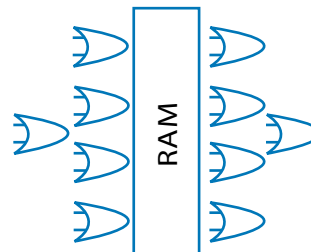


Figure 3: TetraMAX Delivers High Test Coverage on a Wide Range of Design Styles.

Memory Shadow Testing

Logic with fault effects which pass into a memory element and logic that requires the outputs of the memory to set up a fault, are said to be “in the shadow” of the memory. Typically, the memory’s shadow affects a significant portion of the chip and causes a reduction in fault coverage. TetraMAX supports behavioral models of the memories to resolve the shadow effects and increase overall fault coverage for the circuit.

ATPG Design Rule Checking

TetraMAX’s design rule checker (DRC) identifies chip-level test issues. Violations can be analyzed by viewing them directly on the circuit using TetraMAX’s integrated graphical schematic viewer, and detailed violation information is available with context sensitive help. TetraMAX’s fast DRC checks for the following problems:

- Flip-flops which violate scan chain design rules
- Asynchronous logic which may increase ATPG run time or reduce fault coverage
- Clock generation logic and three-state busses that may be difficult to control during ATPG
- Test protocols which may cause incorrect behavior on the tester

TetraMAX’s DRC supports full-scan and partial-scan test methodologies using mux-scan, clocked-scan, level-sensitive scan design (LSSD) and proprietary schemes. For maximum flexibility, TetraMAX accepts user-defined constraints and initialization vectors required for proper scan chain shifting. Complete support is provided for designs with IEEE 1149.1 internal scan shifting protocols and related techniques that minimize the number of external I/O pins required for ATPG.

Vector Compaction

TetraMAX uses the most advanced compaction techniques to minimize test vector count during the ATPG process, even on designs that have many clock domains. With these techniques, TetraMAX reduces the number of test cycles required to test each device, resulting in lower tester costs.

At-Speed Testing

Too many manufacturing defects are timing-related and may not be caught without additional at-speed testing that specifically targets delay defects. With the TetraMAX DSMTest option, designers and test engineers can easily develop test patterns that target the two most widely accepted timing-related defect models: transition faults and path delay faults. This combination provides the highest test coverage of both point and distributed defects that prevent a device from correctly operating at its rated speed. Advanced features unique to the TetraMAX DSMTest option:

- PrimeTime® interface selects critical timing paths and timing exceptions
- Full support for on-chip clocking such as PLLs
- Easy-to-use flow with graphical support for analysis and debug
- ATPG algorithms are optimized for each specific delay testing mode
- Vector merging maximizes delay testing efficiency
- Tester-ready patterns with complete timing

IDDQ Testing

IDDQ testing is a method for enhancing the quality of IC tests by measuring the power supply current of a CMOS circuit. Defect-free CMOS circuits draw very low levels of current during a quiescent state. IDDQ levels are typically an order of magnitude higher in the presence of a silicon defect. IDDQ testing targets

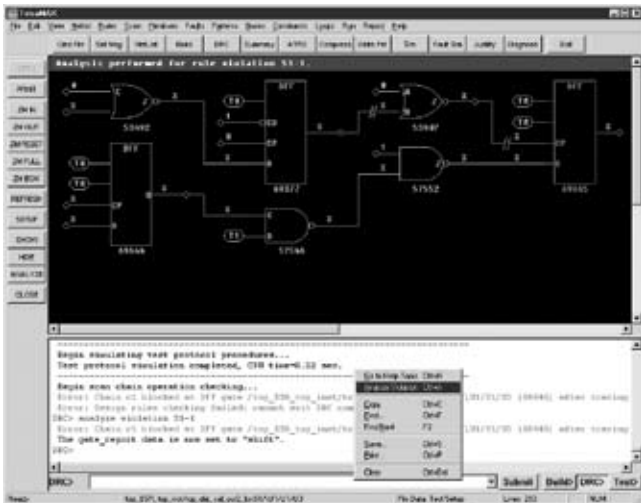


Figure 4: TetraMAX Provides High-Performance ATPG and Advanced Debug Capabilities through its Integrated Graphical Interfaces.

physical defects that create a conduction path from the power supply to ground and result in excessive current draw.

TetraMAX generates a minimal set of high fault coverage vectors for IDDQ testing purposes, and constrains the test vectors to avoid excessive current during the quiescent state. The TetraMAX IddQTest option then accurately validates these vectors for low quiescence using Synopsys VCS™ or other Verilog simulator, thereby ensuring the IDDQ vectors will work on the ATE.

Distributed Processing

For very large designs, the TetraMAX TenX option enables ATPG and fault simulation to be run across multiple processors. The TenX distributed processing architecture is highly scalable to over 10 processors, and compared to a single processor can generate test vectors in less than 1/10th time but with the same high test coverage and minimal vector counts. The TenX option supports networks with heterogeneous platforms and popular compute management applications such as LSF.

Yield Diagnostics

In addition to identifying defective parts from manufacturing, TetraMAX ATPG can also isolate the location of defects on devices that fail TetraMAX test vectors. Automatic and accurate defect isolation is an important step to diagnose critical

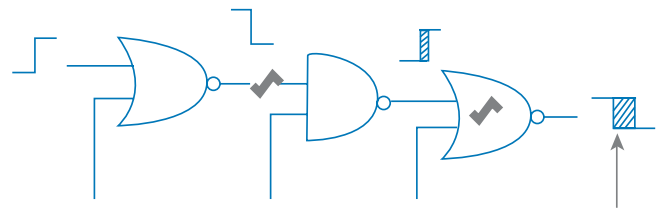


Figure 5: TetraMAX DelayTest Automates testing of Critical Paths.

yield issues, both during production ramp as well as in volume manufacturing. TetraMAX diagnostics read the test vectors and tester failure data, which are the differences between measured and expected responses to those test vectors, and report the fault candidate locations that most likely explain the faulty device behavior observed on the tester. TetraMAX diagnostics use advanced heuristics and a high performance fault simulator for rapid and reliable results in a volume manufacturing environment.

Netlist Formats, Testbenches, and Test Vectors Interfaces

TetraMAX supports popular industry standards for netlist and test vector formats:

Circuit netlist:	Verilog, VHDL (87 and 93)
Library:	Verilog functional (Structural and UDPs)
Testbench:	Verilog (serial and parallel), VHDL-93 (serial only)
Test vectors:	STIL, WGL, Toshiba TSTL2, Texas Instruments TDL91, Fujitsu FTDL, and Verilog VCDE (input only)

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.

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