TetraMAX ATPG  
Automatic test pattern generation

Overview
TetraMAX® ATPG automatically generates high quality manufacturing test vectors. TetraMAX is the only ATPG solution optimized for a wide range of test methodologies that's integrated with Synopsys' DFT Compiler, the leading test synthesis tool. The unparalleled ease-of-use and high performance provided by TetraMAX allows RTL designers to quickly create efficient, compact tests for even the most complex designs.

Key Benefits
- Increases product quality with generated test vectors for high defect detection
- Reduces testing costs through the use of advanced vector compaction techniques
- Increases designer productivity by leveraging integration with Synopsys DFT Compiler
- Creates tests for complex and multi-million gate designs

Features
- Extremely high capacity and performance
- Integrated graphical user interface
- Integrated context-sensitive online help
- Comprehensive scan design rule checking
- Utilizes existing Verilog simulation libraries
- DelayTest option supports testing for timing related defects
- IddQ Test option available for additional fault model support
- PatternMap option reuses existing memory and module-level tests
- Integrated fault simulator for functional vectors

Figure 1. Integrated Test Flow Using TetraMAX ATPG.
Testing Complex ASICs

With TetraMAX ATPG, designers can generate high quality manufacturing test vectors without compromising on high-performance design techniques. While such techniques may impede older generation ATPG tools, TetraMAX is able to produce high test coverage on the resulting complex logic.

TetraMAX supports internal three-state busses including implementations with pull-ups, pull-downs and charge storage. Similar to three-state busses, bi-directional I/O pads are also supported. To ensure ATE (automatic-test-equipment) requirements are met, TetraMAX provides a number of options to generate contention-free vectors for three-state logic.

Memory Shadow Testing

Logic with fault effects which pass into a memory element and logic that requires the outputs of the memory to set up a fault, are said to be “in the shadow” of the memory.

Typically, the memory’s shadow affects a significant portion of the chip and causes a reduction in fault coverage. TetraMAX supports behavioral models of the memories to resolve the shadow effects and increase overall fault coverage for the circuit.

ATPG Design Rule Checking

TetraMAX’s design rule checker (DRC) identifies chip-level test issues. Violations can be analyzed by viewing them directly on the circuit using TetraMAX’s integrated graphical schematic viewer, and detailed violation information is available with context sensitive help. TetraMAX’s fast DRC checks for the following problems:

- Flip-flops which violate scan chain design rules
- Asynchronous logic which may increase ATPG run time or reduce fault coverage
- Flip-flops on clock domains that should be grouped together for proper scan shifting
- Clock generation logic that may be difficult to control during ATPG

TetraMAX’s ATPG supports full-scan, near-full-scan and partial-scan test methodologies using mux-scan, clocked-scan, level-sensitive scan design (LSSD) and proprietary schemes. For maximum flexibility, TetraMAX accepts user-defined constraints and initialization vectors required for proper scan chain shifting. Complete support is provided for designs with IEEE 1149.1 internal scan shifting protocols and related techniques that minimize the number of external I/O pins required for ATPG.
Vector Compaction
TetraMAX uses the most advanced compaction techniques to minimize test vector count during the ATPG process, even on designs that have many clock domains. Static compaction techniques may be used following the completion of ATPG to further compact the test vectors. With these techniques, TetraMAX reduces the number of test cycles required to test each device, resulting in lower tester costs.

Delay Fault Testing
Too many manufacturing defects (up to 50%) are timing-related and may not be caught without additional testing that specifically targets delay defects. With the TetraMAX DelayTest option, designers and test engineers can easily develop test patterns that target the two most widely accepted timing-related defect models: transition delay faults and path delay faults. This combination provides the highest test coverage of both point and distributed defects that prevent a device from correctly operating at its rated speed. Advanced features unique to the TetraMAX DelayTest option:
- PrimeTime® interface selects critical timing paths
- Easy-to-use flow with graphical support for analysis and debug
- ATPG algorithms are optimized for each specific delay testing mode
- Vector merging maximizes delay testing efficiency
- Tester-ready patterns with complete timing

IDDQ Testing
IDDQ testing is a method for enhancing the quality of IC tests by measuring the power supply current of a CMOS circuit. Defect-free CMOS circuits draw very low levels of current during a quiescent state. IDDQ levels are typically an order of magnitude higher in the presence of a silicon defect. IDDQ testing targets the physical defects that create a conduction path from the power supply to ground that results in excessive IDDQ.

With the IddQTest option, TetraMAX generates a minimal set of high fault coverage vectors for IDDQ testing purposes, and constrains the test vectors to avoid excessive current during the quiescent state. IddQTest then accurately verifies these vectors for low quiescence using Synopsys VCS® or other Verilog simulator, thereby ensuring the IDDQ vectors will work on the ATE.

Embedded Memory/Module Testing
The TetraMAX PatternMap option provides the ability to automatically import user-created test patterns for embedded memories and modules. For designs with many small memories, PatternMap provides area savings, and results in more efficient tests compared to memory BIST.
Designers simply supply a set of memory specific test patterns to TetraMAX, which then examines the embedded memory at the chip level. By analyzing the surrounding logic, TetraMAX determines how to appropriately “map” the original memory test patterns to corresponding scan patterns. These scan patterns can then be applied at the tester, thereby testing the embedded memories.

**Fault Simulation**
TetraMAX FaultSim simulates and grades existing sets of functional vectors. FaultSim uses a high-performance algorithm to obtain optimum results for large circuits and requires dramatically less memory than traditional fault simulation tools. Fault simulation may be run stand alone on functional vectors and the fault coverage results can be combined with ATPG fault coverage results to provide comprehensive coverage reports. FaultSim is included with TetraMAX and is also available as a separate standalone tool.

**Netlist Formats, Testbenches, and Test Vectors Interfaces**
TetraMAX supports popular industry standards for netlist and test vector formats:
- **Circuit netlist**: Verilog, VHDL (87 and 93), and EDIF
- **Library**: Verilog functional (structural and UDPs), TestGen™ (source)
- **Testbench**: Verilog (serial and parallel), VHDL-93 (serial only)
- **Test vectors**: STIL, WGL, Toshiba TSTL2, Texas Instruments TDL91, Fujitsu FTDL, and Verilog VCDE (input only)