Visual Elite

Advanced TLM-RTL Design and Integration Platform

Continuous Design Flow from TLM to RTL

Visual Elite™ is the state-of-the-art design and integration platform enabling designers and system architects to intuitively capture and connect SystemC and HDL blocks into complex SoC’s and systems. Visual Elite is built upon a strong HDL implementation infrastructure while offering the most advanced electronic system-level (ESL) and transaction level modeling (TLM) concepts and mechanisms. Visual Elite greatly simplifies and accelerates capturing design structures in a hierarchical manner from untimed algorithm systems and TLM architectures down to HDL descriptions. Such design and integration platform across abstraction levels and domains is key in managing design complexities and disciplines throughout the design life-cycle.

Accelerates Design Creation

Visual Elite offers a variety of languages and design entry methods allowing the user to select the best suited approach for their modeling needs. Visual Elite supports both text-based and graphical entry, including block diagrams, state diagrams and connectivity tables. Designers can use VHDL, Verilog, SystemC or any combination of these to design and build products.

Facilitates TLM Platform Assembly and Prototyping

Visual Elite facilitates TLM platform construction using graphical block diagram and communication channels while substantially reducing coding efforts. Visual Elite provides Virtual Platform automation using pure un-timed and TLM functional models to establish an early HW/SW verification flow. Once a TLM platform is verified, Visual Elite generates SystemC executable, with an ISS or HOST communication interface, that can be linked with application software. Such virtual hardware platform can be distributed to software development and test teams very early in the design process, well in advance of physical hardware availability.

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Intuitive Authoring Environment

Visual Elite provides state-of-the-art mixed-language authoring environment. All graphical tools are based on native language semantics enabling use of the complete language set.

Modeling methods start from high-level un-timed TLM blocks down to a unique set of macros for data flow design, supporting VHDL/Verilog/SystemC. These data flow elements allow on-the-fly function re-configuration while substantially reducing logic manipulation coding.

Manages Design and Collaboration

Visual Elite allows distributed design teams efficient control and management of the entire design process. Built-in documentation and reuse features, such as text-to-graphics transformation, simplify design management. The design infrastructure for data and project management enables team leaders to enforce a consistent design flow and methodology. The documentation capability enables chip architects and designers to share ideas and design requirements, including hierarchical views within HTML, and links into Microsoft OLE and FrameMaker.

Design Validation

Visual Elite offers intuitive design representations allowing designers to review the design and identify problems even before detailed simulation. During simulation, Visual Elite can plug with any standard simulation engine and users can interactively animate model execution and use a unique cause and effect system that pinpoints bugs from the waveform and annotates them back to the design source.

Design Flow Integration

Visual Elite can link with existing mixed-language designs and offer cross language model distribution, including mapping SystemC RTL into HDL. Model generation can be tailored to various SystemC and HDL synthesis tools and allow single source modeling. Visual Elite supports custom modules from tools such as SPW, Matlab, and popular FPGA core libraries.

Integrates with Vista and System Architect

Visual Elite is integrated with Vista™ and System Architect™ offering a comprehensive design flow for integrating, debugging and exploring SystemC and TLM platforms.

To learn more about Visual Elite contact Mentor Graphics or visit our website for product news and information.