Tessent Memory Test
Solutions for Embedded Memory Self-Test, Repair, and Debug

Industry Leading Solution for Memory Built-In Self-Test
Mentor Graphics Tessent® MemoryBIST provides a complete solution for at-speed testing, diagnosis, repair, debug, and characterization of embedded memories. The solution’s architecture is hierarchical, allowing BIST and self-repair capabilities to be added to individual cores as well as at the top level.

On-chip generated test patterns are delivered to the memories at application clock frequencies. The Tessent MemoryBIST controllers are configurable to support a variety of memory types, as well as a range of memory timing interfaces and memory port configurations. The controllers are accessed and controlled through the test access port (TAP) interface using IEEE 1149.1 and IEEE 1500 protocols. The controllers can be accessed throughout the life of the integrated circuit, including manufacturing test, silicon debug, and system verification.

Tessent MemoryBIST includes a unique comprehensive automation flow that provides design rule checking, test planning, integration, and verification all at the RTL or gate level. The back-end flow for memory test (debug and characterization) is managed by Tessent SiliconInsight® Memory, an interactive, desktop-based debug environment.

Hard Algorithm Programmability
At design time, one or more Mentor-provided or user-developed memory test algorithms can be hard-coded into a Tessent MemoryBIST controller. Any of these

Key Benefits
- Self-test and self-repair IP integration, as well as reuse of embedded memory test inserted cores, shorten time-to-market.
- Design-time algorithm specification allows for quality improvement and test time optimization.
- Field algorithm specification provides full control of quality and test time trade-offs.
- Built-in row- and column-based repair analysis reduces test time for repairable memories.
- Single insertion memory repair on any tester reduces manufacturing costs.
- Desktop-based test debug and characterization speeds time to market.

Key Features
- Design-time algorithm specification supports hardcoding of custom test algorithms. Innovative architecture supports the programming of any test algorithm.
- Field algorithm specification supports run-time downloading of custom test algorithms. Full automation provided for downloading program code through the TAP or CPU interface.
- On-chip global eFuse management includes fuse data compression and programming.
- On-chip test and repair supports third-party repairable SRAMs.
- Self-repair supports any number of power domains distributed across any number of physical blocks.
- Supports any level of parallelism for both test and repair activities.
algorithms can then be applied to each memory through run-time control. This capability is useful for optimizing test time by selecting shorter test algorithms as the manufacturing process matures. The hard programming feature includes the following capabilities:

- High-level programming language for straightforward algorithm specification.
- Access to a large library of common memory test algorithms.
- Library of algorithm program code is included for direct use or as a reference for creating modified algorithms.

Field Programmable Option

The Tessent MemoryBIST Field Programmable option allows any memory BIST controller to include full run-time programmability. With this feature implemented, any user-programmed memory test algorithm can be downloaded into the BIST controller while on the tester or in system. This capability allows any unforeseen defect mechanism to be dealt with without a design respin. Both the hard and soft programming features can be used within the same BIST controller.

Field algorithm programming:

- Supports the run time (post-silicon) programming of custom test algorithms.
- Provides automation for downloading program code through the TAP or specified CPU interface.
- Supports a combination of both hardcoded algorithms and microcode memory for post-silicon algorithm programming within a single memory BIST controller:
  - Allows default run without scan initialization.
  - Useful for learning during yield ramp because different diagnostic algorithms can be downloaded as needed.
- Useful for production/board/system reuse because default algorithm requires no external initialization data.

Power-Aware Self-Repair Option

The Tessent MemoryBIST repair option eliminates the complexities and costs associated with external repair flows. It tests and permanently repairs all defective memories in a chip using virtually no external resources. The Tessent MemoryBIST self-repair architecture supports the standard approach of using a centralized pool of programmable fuses to store memory repair info. During memory test, the built-in repair analysis engines within each BIST controller calculate the fuse information needed to repair each memory. Fuse information can be accumulated over different test conditions.

The final data is stored in a local self-repair (BISR) register that is part of a single serial chain specific to a power domain. These serial chains are then used by a fuse controller to shift and compress repair data into the central fuse array, as well as to shift data back out to the memories each time a power domain is reactivated. The solution supports any number of power domains and be distributed across any number of physical blocks.

Shared Bus Interface Support

Processor cores from vendors such as ARM can provide a shared bus interface to the memories internal to the processor core IP. This interface provides a standard set of test address, data, and control ports to access all memories embedded within each processor core.

Block diagram of shared bus interface.
The memory BIST controller no longer communicates directly to each memory but must now understand how to gain access to each memory through the common interface signals and, in addition, must account for the different levels of pipelining to and from each memory.

Tessent MemoryBIST supports integrating memory BIST and repair capabilities into a design that contains both stand-alone memories and memories embedded within an IP core that are only accessible through a shared bus interface.

### 3D-IC Support

Tessent MemoryBIST provides support for the rapidly growing use of 3D packages consisting of one or more memory die stacked on top of a separate logic die.

The memory BIST control logic is integrated into the logic chip, maximizing real estate for memory cells and allowing at-speed testing of the memory bus logic and connections.

Both bond wire and through-silicon via (TSV)-based interconnects can be tested. The shared bus interface support also enables testing package configurations in which multiple memory die are stacked and connected to a single logic die via the same electrical interconnects. The field programmability supports changes in the memory die, or variant stacks that use different memory designs.

### Test Debug and Characterization

Tessent SiliconInsight Memory provides a desktop-based interactive debug and characterization system. Designers can execute tests, collect data, and generate shmoo plots for any selection and order of BIST-tested blocks on the device. Tessent SiliconInsight can greatly increase productivity during silicon validation and debug, speeding time-to-market.

![The Tessent SiliconInsight interactive environment.](image)

### Tessent Silicon Test and Yield Analysis Solutions

Tessent MemoryBIST is part of the Mentor Graphics industry- and technology-leading tool suite for silicon test and yield analysis. The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on UNIX and Linux. For more information, visit www.mentor.com.

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