Tessent FastScan
Advanced Automatic Test Pattern Generation

Interface for viewing and correcting testability problems.

Industry Leading ATPG
Mentor Graphics Tessent™ FastScan™ is an automatic test pattern generation (ATPG) solution with a wide range of fault models, comprehensive design rule checks, extensive clocking support, and innovative algorithms for performance-oriented pattern compaction. It simplifies the process of generating high-coverage test sets. Its ability to be applied to most any type of design makes it the most versatile ATPG solution available.

At-Speed Testing
Current fabrication processes result in a population of speed-related failures that require detection through advanced test techniques. A comprehensive at-speed test solution is critical to ensure high-quality test. Tessent FastScan’s at-speed solution includes transition, multiple detect transition, timing-aware, and critical path testing.

Transition testing looks for delays on nodes at each gate, targeting the entire design for speed-related defects. Tessent FastScan’s critical-path analysis capabilities generate robust sequential patterns to detect defects along a design’s critical paths. Timing-aware patterns are similar to transition patterns but they use SDF timing information to target faults along the longest paths.

Key Benefits
- Delivers high performance ATPG for designs with structured scan.
- Reduces run time with no effect on coverage or pattern count using distributed ATPG.
- Maximizes test coverage by minimizing the impact of Xs caused by false and multi-cycle paths.
- Identifies testability problems early using comprehensive design rule checking.
- Reduces test validation time with automatic simulation mismatch debugging.
- Ensures shorter time to market with integration into all design flows and foundry support.
- Mentor Graphics award-winning customer support. ensures success.

Key Features
- Extensive fault model support, including stuck-at, IDDQ, transition, path delay and bridge.
- On-chip PLL support for accurate at-speed test.
- MacroTest option automates testing small embedded memories and cores with scan.
- Supported in the Tessent SoCScan hierarchical silicon test environment.
Tessent FastScan supports the use of on-chip PLLs for delivering accurate at-speed clock edges. With input on the clocking procedures for the PLL, it can generate accurate at-speed tests using the design’s on-chip clocks.

Tessent FastScan reduces the effect that unknown states (Xs) have on test coverage by intelligently handling false and multicycle paths.

**Test Pattern Compaction**

Tessent FastScan is known for delivering high-coverage, compact test sets. However, with the growing need to improve test quality and with at-speed patterns becoming a standard, the amount of test data can still be an issue. In cases where test data volumes exceed automatic test equipment limits or vendor requirements, Tessent TestKompres® and embedded deterministic test (EDT) offer a unique solution. Because both products share the same efficient ATPG engine, the migration to compression is simplified.

**Testability Analysis and Debug**

A visual debug utility is integrated within Tessent FastScan for viewing and correcting testability problems. Visualizer presents the design in various views such as schematic, design structure, waveform, library, data, hierarchy, and additional views to facilitate viewing and troubleshooting.

The intuitive interface built into Visualizer also allows viewing of the session transcript which includes active links for design rule violations, logic displays, file editing, documentation, and gate callouts. ATPG statistics reporting provides detailed analysis of untestable faults and classifies them into recognizable categories that simplify the debugging of low test coverage issues.

**Hierarchical Logic Test Strategy with Tessent SoCScan**

Tessent FastScan can be used with Tessent SoCScan to take advantage of the Mentor Graphics automated hierarchical test integration and test generation flow. Tessent SoCScan makes use of shared isolation and capture-by-domain technologies to deliver independent core-level ATPG and chip-level pattern reuse. Tessent SoCScan also provides access to BurstMode technology for higher at-speed test coverage and improved power management.

**Tessent Silicon Test and Yield Analysis Solutions**

Tessent FastScan is part of the Mentor Graphics industry- and technology-leading tool suite for silicon test and yield analysis. The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on UNIX and Linux. For more information, visit www.mentor.com.