Eldo RF
High-Performance RF IC Verification

Key Benefits
• Full-chip RF IC verification for wireless applications
• Seamless integration into Mentor and other leading IC design flows
• Superior support quality—Mentor Graphics has the only 5-Star support in EDA

Key Features
• Closed-loop phase noise analysis for PLLs and frequency synthesizers
• Multi-tone steady-state analysis for large RF IC designs containing thousands of elements
• Modulated steady-state analysis with RF/baseband partitioning
• Library of digitally modulated sources for all wireless standards
• Strongly non-linear signal analysis
• Built-in optimization capability.
• System-level simulation capability using Verilog-A

FOR THE MOST CHALLENGING TELECOM AND WIRELESS DESIGNS
Facing the explosive growth of mobile communication and wireless products, RF IC designers are given the daunting task of analyzing and fully verifying the most critical part—the RF section. Time-to-market pressures and steadily increasing levels of integration and complexity call for new high-performance and high-capacity RF IC verification tools.

EXTENDING MIXED-SIGNAL SIMULATION TO THE RF DOMAIN
Eldo® RF provides the necessary performance and capacity breakthroughs for RF IC simulation, taking the baton where existing tools reach their limits. Consistently extending the capabilities of Eldo, the Mentor Graphics best-in-class analog simulator, Eldo RF provides a set of dedicated algorithms to accurately and efficiently handle the multi-GHz signals in modern wireless communication applications.
RF ANALYSIS CAPABILITIES

Steady-State Analysis
Steady-state analysis of RF IC circuits excited with single-tone or multi-tone large signal sources is easy with Eldo RF. Multi-tone steady-state analysis allows you to quickly analyze amplifiers, filters, and mixers. Analysis features automate computation of intermodulation products, compression points, intercept points, and extraction of large-signal S parameters.

Steady-State Small Signal Analysis
A number of small-signal analysis such as the steady-state small signal (SSTAC) analysis or the steady-state transfer function (SSTXF) analysis complement the steady-state core algorithm. They are used to easily predict frequency responses when frequency translation occurs due to a mixing operation for example, and regular small signal analysis (AC) is not applicable.

Steady-State Noise Analysis
Steady-state noise analysis determines the output noise spectrum and the noise figure, with results sorted by the individual contribution of every noisy device. Eldo RF has the remarkable capability that non-linear noise analysis can be performed under large signal multi-tone conditions, which is mandatory for the accurate simulation of mixers.

Oscillator and Phase Noise Analysis
Eldo RF computes the steady-state response of circuits containing multiple oscillators or voltage-controlled oscillators in a fraction of the time needed by transient-based methods. Other fundamental frequencies are allowed, so large signal analysis of combinations such as VCO and mixer are easy to analyze. You don’t need to worry about the start-up conditions or the oscillator because everything is computed in the frequency domain. Phase noise and amplitude noise are easily and accurately analyzed, using proprietary algorithms, which yield accurate results both close to and far from the carrier. Sorted contributions of each and every element is available in tabular formats. Time domain period and long-term jitter information is also available, for both forced and non-forced circuits.

Eldo RF steady-state PLL partitioned algorithm predicts spurious in output spectrum and closed-loop transistor-level phase noise.
Frequency Dividers
Eldo RF supports the analysis of frequency dividers combined with voltage controlled oscillators. Phase noise can also be predicted at the output of the dividers. Eldo RF is the only tool to accurately predict the phase noise at intermediate division stages, due to its unique handling of noise correlation. A very handy frequency divider macro-model is available for architectural exploration.

Modulated Steady-State Analysis
To accurately predict effects such as adjacent channel power ratio, Eldo RF supports a dedicated algorithm that handles modulated signals. A time-varying spectrum is computed by this algorithm, which basically merges the steady-state and the transient algorithms, decoupling the resolution of the RF carriers from the slow-varying modulation information. Eldo RF can also use the MODSST algorithm for some partitions (typically, the RF blocks) and regular transient algorithm for the rest of the circuit (typically, the baseband blocks). The speed up provided by this algorithm may reach one or two orders of magnitude over brute force transient simulation, with no loss of accuracy. A variety of standard outputs such as IQ trajectory diagram, constellation diagram, or Eye diagram is available.

Digitally Modulated Sources
To accommodate different wireless standards, Eldo RF supports all common digital modulation formats, such as GMSK, QPSK, QAM, GFSK, EDGE, OFDM, etc. Built-in sources deliver signals modulated according to these schemes, including the standard baseband filters such as Root Cosine or Gaussian filters. The input signal can be either explicit binary sequences, or CCITT-compliant PRBS sequences. Arbitrary IQ modulators can also be used, which read the IQ information from external user-defined tables.

Parametric Sweeping
Take advantage of efficient parametric sweeping to vary signal power, fundamental frequencies, temperature, power supply level, component values, or any parameterized value for a complete verification of RF IC designs. Efficient parametric sweeping is critical for many RF simulations such as compression points or intermodulation, and the algorithms in Eldo RF are extremely well-suited for that purpose, thus maximizing designers productivity.
DEDICATED BUILT-IN RF MEASUREMENTS

Eldo RF Speaks the Language of RF Designers

A set of RF-dedicated functions plus a powerful post-processing measurement and extraction language allow full customizations, making RF characterization easy. The following standard RF measurements are supported:

- 1dB compression points
- Nth-order intercept points
- Nth-order intermodulation products
- Mixer conversion gain
- SSB and DSB noise figure
- Minimum noise figure
- Gamma opt
- Input and output stability circles
- Gain and power circles
- Impedance/admittance locus vs. frequency
- Large-signal S parameters
- K, B and MU factors
- Total harmonic distortion
- Power-added efficiency
- Period jitter
- Long-term jitter.

PHASE-LOCKED-LOOP ANALYSIS

Steady-State

Eldo RF contains a dedicated algorithm for the analysis of the steady-state behavior of PLLs. The analysis of PLLs is a difficult problem for classical transient simulation, because the time constants at stake differ by several orders of magnitudes. The bandwidth might be a few 100 kHz whereas the VCO oscillates at several GHz. Unfortunately, transient simulation has to follow the fastest signal, and thus the number of computed time points is prohibitive, leading to days or weeks of simulation, even on the most powerful computers.

To overcome this difficulty, the Eldo RF steady-state PLL algorithm partitions the design and uses a global convergence loop to directly compute the steady-state solution (i.e., the locked state). The gain in CPU time is spectacular (typically 50X); and even better, the results are more accurate than the solution provided by the transient simulation. This is a rare case in which a clever algorithm provides both a spectacular speed up and higher accuracy. Usually, you have to accept a trade-off between speed and accuracy, using either fast-spice or behavioral modeling techniques. The steady-state waveforms allow analyzing the spurious in the output spectrum, directly in the frequency domain; thus, the
tedious post-processing FFTs of transient waveforms are completely avoided.

**Closed-Loop Phase Noise Analysis**
The Steady-State PLL algorithm in Eldo RF can also compute the closed-loop phase noise spectrum out of the PLL, using a partitioning strategy for accelerated convergence. All noise sources are taken into account, without any simplifications, because the input is a plain transistor-level netlist. All building blocks, such as phase-frequency detector, charge pump, divider, and VCO, operate as non-linear elements. All transistor device models are supported, and no behavioral modeling or linearization is necessary. A key feature of the algorithm provides the individual contributions of the building blocks to the global output phase noise.

**Delta Sigma Synthesizers**
Although it is not possible to include a transistor-level description of a delta-sigma converter in the case of fractional delta-sigma synthesizer (because there is no steady-state solution), it is still possible to inject a phase noise source representing the delta-sigma noise to see its impact on the global output phase noise.

**FITTING STANDARD IC DESIGN ENVIRONMENTS**
**Best-In-Class Analog Simulation Included**
Eldo RF includes all the capabilities of the Mentor Graphics prominent analog transistor-level simulator, Eldo. It supports all industry-standard transistor models, and benefits from strong foundry support. Device models include BSIM3/4, BSIM, MM9, MM11, PSP, HiSIM, GP, HICUM, VBIC, MEXTRAM, Curtice, Statz, as well as user-defined models. Most importantly for the RF designer, large-signal S parameters can be extracted, and multiple lossy transmission lines are supported. Eldo RF also supports the W elements.

**Mentor’s Design Architect IC Integration**
Eldo RF is integrated with the Mentor Graphics’ Design Architect® IC™ product for analog and mixed-signal design. A complete simulation interface in Design Architect IC controls the simulation set up and the netlisting process. Simulation results may be

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The modulated steady-state analysis is a mixed time/frequency analysis. It computes a time-varying spectrum, allowing much larger timesteps compared to brute force transient simulation.
analyzed using the EZwave™ waveform viewer, with the help of a powerful schematic cross-probing facility. Design Architect IC provides links with the industry-standard Calibre® and Calibre xRC™ tools, allowing post-layout simulation including parasitic elements with Eldo RF.

**Cadence Integration**
Eldo RF is also integrated in the Cadence® Analog Design Environment through the Artist Link layer provided at no charge by Mentor Graphics. Simulation set up, direct netlisting, waveform processing, and cross-probing are fully supported.

**Powerful Waveform Post-Processing**
The Mentor Graphics standard EZwave waveform processor provides the advanced features needed to operate on RF, low-frequency baseband analog, and digital signals. It manipulates data in both the frequency and time domains. Smith charts, Eye diagrams, FFT with sophisticated windowing, or signal-to-noise calculation are just some of the built-in features.

**MULTI-THREADED FREQUENCY ALGORITHMS**
Delivering Outstanding Performance
Eldo RF uses a high-performance multi-threaded algorithm that incorporates advanced numerical analysis techniques (XCT, Krylov-Newton, and Harmonic Balance). Operating in the frequency domain, it gracefully and efficiently handles difficult circuits with multi-tone inputs, distributed elements or high-Q elements, when time-domain algorithms such as the shooting method use to fail or perform poorly. These algorithms are well-suited for parallel operation on multi-CPU machines. Eldo RF multi-threading operation does not require any additional license. With circuits containing several thousands of transistors, Eldo RF routinely demonstrates a 10X to 100X speed improvement compared to time-domain based simulators, with superior accuracy.

Simulation of close strong interferers is extremely fast, as the algorithms are not sensitive to the relative spacing of the input and output frequencies. You are completely free to choose the amplitudes and frequencies of the signals, so that you can verify the genuine specifications. Also, the intrinsic accuracy of the algorithms is ideal for the analysis of signals with widely different scales. Simulating signals with -150 dB dynamic range is a routine task with Eldo RF.
DESIGN OPTIMIZATION
Powerful Built-in Optimizer Included

Eldo RF incorporates powerful optimization algorithms to assist the designer in the fine tuning of circuit performances. The optimization facility does not require any external tool. It is all integrated in the simulation kernel for maximum efficiency. It supports continuous and discrete, constrained or unconstrained parameters, and concurrent optimization of several simulations and analyses. Complete curve fitting is also available. Use of the optimizer is particularly efficient for nominal performance optimization of gain, matching networks, power dissipation, IP3, etc., when the design parameters are strongly coupled and simple sweeping is inconvenient or impractical. Another ideal application is “process retargeting,” when a design must be ported from one technology to the next-generation technology and the performance must be maintained.

SYSTEM LEVEL SIMULATION WITH VERILOG-A
Analog Behavioral Simulation

When the size of the circuit is such that transistor-level simulation is too slow, using analog behavioral modeling can be an effective methodology to reduce the CPU time. To that end, the Verilog-A option of Eldo RF supports an arbitrary mix of Verilog-A descriptions and transistor-level SPICE netlists. The models can be used with all analyses based on steady-state analysis and most importantly, for modulated steady-state as well. Low noise amplifiers, mixers, oscillators, filters, or IQ modulators can be described in Verilog-A to save CPU time when simulating large systems. Using parameterized models also allows efficient architectural exploration, tuning the system performance as required in minutes.