Tessent BoundaryScan
Comprehensive Boundary Scan and I/O Test Solution

Hierarchical Tessent BoundaryScan infrastructure.

Industry Leading Solution for Boundary Scan Integration

Mentor Graphics Tessent® BoundaryScan is a complete solution for the creation and integration of boundary scan cells and related control logic for embedded test and diagnosis of integrated circuit I/Os, as well as test and diagnosis of board-level interconnects between ICs. Tessent BoundaryScan provides a completely automated solution for adding standard boundary scan support to ICs of any size or complexity, reducing IC engineering development effort and improving time-to-market.

Tessent BoundaryScan supports standard 1149.1 boundary scan cells, 1149.1 custom boundary scan cells, and optionally 1149.6 boundary scan cells for differential I/O cells driving AC-coupled nets. It also provides a unique 1149.1-based solution for contactless testing of I/Os.

Access to the boundary scan cells is provided through the Mentor Graphics test access port (TAP) interface using the IEEE 1149.1 (JTAG) and IEEE 1149.6 (ACJTAG) protocols. The boundary scan logic can be accessed throughout the life of the IC, including manufacturing test at all package levels, silicon debug, and system verification. The result is that both I/O cell defects and inter-IC board interconnect problems are detected before shipment, reducing field support costs and increasing customer satisfaction.

Key Benefits

- Ready-to-use library of boundary scan cells, test benches to automate verification in simulation, short test times, and minimal tester hardware requirements reduce IC development costs.
- Quick boundary scan integration, automated rule checking with interactive debug, and quick integration into board test programs shorten time-to-market.
- Detecting IC I/O cell defects and enabling effective testing of inter-IC connections reduce field returns.
- Mentor Graphics award-winning customer support ensures success.

Key Features

- Comprehensive hierarchical RTL integration and verification flow.
- Support for user-defined boundary scan cells including those embedded in sub-blocks or cores.
- Comprehensive contactless testing of I/Os.
- Support for both the IEEE 1149.1 and 1149.6 standards.
- Fully plug-and-play compatible with the complete set of the Mentor Graphics Tessent products and capabilities.
The 1149.1 standard enables fast, effective test of I/O cells and internal logic using low pin-count testers. This reduces test cost while improving yield.

**Automatically Integrate Boundary Scan into Design RTL**

Tessent BoundaryScan automatically generates and integrates the RTL code for the TAP controller and boundary scan cells into the design RTL. It also generates the scripts required for logic synthesis, a BSDL description of the boundary scan functionality, simulation testbenches to verify the boundary scan implementation, and test patterns for manufacturing test.

**IEEE 1149.1 Custom Cell Support**

Tessent BoundaryScan provides support for custom boundary scan cells, including those contained within third-party IP blocks. Custom boundary scan cells can be intermixed with Tessent BoundaryScan–generated scan cells. Tessent BoundaryScan supports custom cell integration and verification and generates a BSDL description of the boundary scan functionality based on a user-supplied library file describing the custom boundary cells.

**IEEE 1149.1-Based Contactless I/O Test**

Reduced-pin-count test, in which many signal pads are not probed, is commonly used for high-pin-count ICs. If the unprobed pads are bi-directional and boundary-scan accessible, then the path to and from each pad can be tested for stuck-at faults. Although DC parametric tests are typically performed, by far the most likely DC parametric test to fail is pin leakage current. Besides being an important pin specification, it is a sensitive indicator of the IC’s reliability.

The Tessent BoundaryScan solution provides a comprehensive set of I/O tests that are delivered without having to contact the I/Os. The tests include a structural wrap-around test, accurate measurement of both the positive and negative leakage currents (IIH and IIL), and a tri-state enable test. All tests can be applied to any number of I/O in milliseconds. This solution not only drastically reduces the time needed to test I/Os but also allows for a reduced pin count and/or multi-site test methodology. The approach can also improve yield as it avoids possible contact resistance issues and load-board leakage/noise problems.

**Optional IEEE 1149.6 Support**

The Tessent BoundaryScan AC option provides support for adding 1149.6 boundary scan to differential I/Os that drive AC-coupled nets at the board level. The 1149.6 standard is required because 1149.1 assumes DC input levels, DC threshold voltages, and no noise. None of these characteristics is true for differential, AC-coupled nets. However, the 1149.6 standard is completely compatible and compliant with the 1149.1 standard, so the same boundary scan implementation can link together boundary scan cells from both standards.

**Tessent Silicon Test and Yield Analysis Solutions**

Tessent BoundaryScan is part of the Mentor Graphics industry- and technology-leading tool suite for silicon test and yield analysis. The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on UNIX and Linux. For more information, visit www.mentor.com.