Tessent TestKompress
ATPG with Embedded Compression

Industry Leading Scan Test Tool
The Mentor Graphics Tessent® TestKompress® industry-leading automatic test pattern generation (ATPG) solution delivers the highest quality scan test with the lowest manufacturing test cost. The foundation of Tessent TestKompress is the industry-proven ATPG engine that is able to apply all the fault models necessary for thorough silicon test.

Reduced Test Time
The patented embedded deterministic test (EDT) technology incorporated into Tessent TestKompress reduces both test time and data volume without any loss in test coverage. Consistent compression levels, regardless of design architecture are achieved by effective X masking without the need for X bounding, test points, or any other design modifications.

The main components of EDT logic (decompressor and compactor) are part of the scan path only, so functional timing closure is not affected. EDT logic can be generated in all design flows and is independent of synthesis tools. The EDT logic can be added at a design’s top level or used in a modular configuration by placing the decompressor and compactor into each block of the design.

Highest Coverage for Advanced Designs
Tessent TestKompress uses industry-proven fault models to uncover the most subtle defects. The tool supports standard stuck-at fault models for targeting static failures as well as the necessary advanced fault models such as transition models for uncovering dynamically activated defects. Bridges and opens can be specifically targeted by advanced fault models intended for small geometry designs. It supports accurate at-speed clock edges and both launch-off-shift and capture transition fault application.

Key Benefits
• Provides thorough testing of digital logic with scan-based patterns.
• Reduce both test time and data volume as much as 100X.
• Provides fast pattern generation through high-performance ATPG and distributed processing.
• Mentor Graphics award-winning customer support ensures success.

Key Features
• A wide variety of fault models, including stuck-at, transition, path delay, and multiple-detect provide a thorough silicon test.
• Supports low pin count test strategies (as few as one scan channel).
• Scan debug environment for quick troubleshooting.
• Tightly integrated with yield diagnosis and analysis tools: Tessent Diagnosis and Tessent YieldInsight™.
• Supported in the Tessent SoCScan hierarchical silicon test environment.

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Tessent TestKompress provides several options to target bridge defects. A multiple detect/N-detect fault model targets bridging faults that result from random particles. Embedded multiple detect (EMD) test can be used without increasing the pattern count. The physical bridge fault model targets feature-dependent bridge defects whose candidates can be directly extracted from the physical layout with Calibre® nmLVS. Timing-aware ATPG can be used to selectively test the most critical paths.

Tessent TestKompress’ X masking capability provides X tolerance while maintaining high test coverage. False and multicycle paths are a major source of X states during at-speed test. X masking intelligently handles these paths by reading the SDC file and masking as necessary, resulting in more effective test coverage, higher levels of compression, and stable patterns on the tester.

Named capture procedures provide a powerful means of supporting the generation of accurate at-speed clock pulses with the on-chip PLL.

**More Efficient Use of Tester and I/O Pins**
Compressed patterns generated by Tessent TestKompress operate the same on the tester as standard ATPG patterns, but with a reduction in test data volume and test time. As few as a single scan channel can be used to ease issues with routing and external I/O. Dual channel configuration capability provides flexibility to support different testers. This is especially useful in manufacturing test flows that use low-pin-count testers or multi-site testing.

**Testability Analysis and Debug**
A visual debug utility is integrated within Tessent TestKompress for viewing and correcting testability problems. Visualizer presents the design in various views such as schematic, design structure, waveform, library, data, hierarchy, and additional views to facilitate viewing and troubleshooting.

The intuitive interface built into Visualizer also allows viewing of the session transcript which includes active links for design rule violations, logic displays, file editing, documentation, and gate callouts. ATPG statistics reporting provides detailed analysis of untestable faults and classifies them into recognizable categories that simplify the debugging of low test coverage issues.

**Hierarchical Logic Test Strategy with Tessent SoCScan**
Tessent TestKompress can be used with Tessent SoCScan to take advantage of the Mentor Graphics automated hierarchical test integration and test generation flow. Tessent SoCScan makes use of shared isolation and capture-by-domain technologies to deliver independent core-level ATPG and chip-level pattern reuse. Tessent SoCScan also provides access to BurstMode technology for higher at-speed test coverage and improved power management.

**Tessent Silicon Test and Yield Analysis Solutions**
Tessent TestKompress is part of the Mentor Graphics industry- and technology-leading tool suite for silicon test and yield analysis. The Tessent suite includes integrated solutions for test insertion; ATPG; on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on UNIX and Linux. For more information, visit www.mentor.com.