EDA Presentation Sheet

## SLED, the Schematic Link EDitor

The reference for mixed-signal, multi-level and multi-domain circuits

SLED is a hierarchical schematic entry solution of the **third generation** allowing designers to perform graphic entry and configuration of their designs in a shorter time. It blends efficiently the feasibility of linking components and of interactively and graphically configuring design contexts for hierarchical netlisting. SLED also improves designers' productivity by enabling creation of true mixed-signal circuits, multi-level and multi-domain systems.

SLED naturally becomes the central element of your schematic driven design flow!

KEY BENEFITS

- ✓ Provides a user friendly interface with high efforts made on ease of use

- ✓ Allows the exchange of files with other schematic entry tools and with other tools in the design chains

- ✓ Supports the most common modeling languages such as SPICE, Verilog, Verilog-A, VHDL and VHDL-AMS

- ✓ Enables modeling of MEMS (Micro Electro Mechanical Systems) and multi-domain systems thanks to graphic VHDL/VHDL-AMS link editing

- ✓ Delivers a dynamic link with the mixed-signal simulator SMASH for schematic driven design
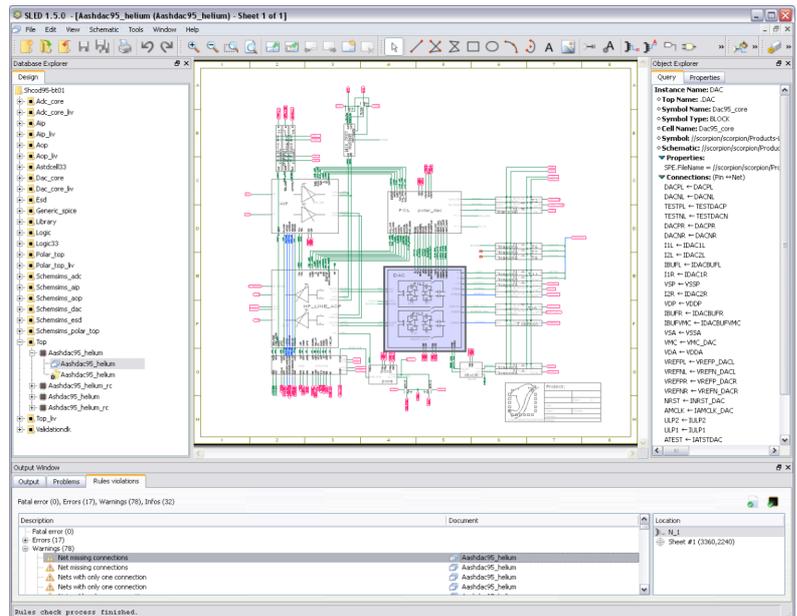
PRODUCT CHARACTERISTICS

The capability for mapping HDL code of any Hardware Description Language graphically throughout the design hierarchy facilitates the creation, orderly assembly, verification and reuse of models for synthesis or simulation.

SLED allows multiple levels of descriptions for system or single block validation, while combining SPICE and HDL representations, to ease architectural design of any System-On-Chip. A system can be iteratively validated by using a SPICE representation of a single block, while all other blocks in the system are represented in HDL for a full functional mixed-signal simulation. It is fundamental for state-of-the-art hierarchical designs of multi-domain components.

For design of analog circuits, the generic library of SPICE components, combined with multi-flavor SPICE netlisting, improves designers' productivity by enabling the creation of true mixed-signal circuits, as state-of-the-art analog designs include hand-crafted logic. The graphic configuration of Design Contexts enables netlisting with the appropriate SPICE flavor respectively for analog simulation, for Schematic Driven Layout (SDL) and for Layout Versus Schematic (LVS) without requiring any change to the schematics.

SLED is available identically under Linux, Solaris and Windows.

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Key features

Compared to some integrated solution, **SLED is both framework independent and open to bridging** with EDA tools for interoperability at different levels of the Design Chains.

Ease of use

✓ Direct syntax colorized behavioral code display to facilitate the reading of HDL and HDL-AMS models.

✓ Easy push/pop navigation through hierarchical schematics.

✓ Click'n drop symbols of any blocks from generic or ad-hoc libraries and drag them while preserving wire connections.

✓ Schematic consistency checks

Save time thanks to early error detection during design with coherency checks, i.e. symbol vs. model I/O, and online Electrical Rule Checks (ERC), i.e. shorted output pins…

Dynamic link with SMASH

SLASH, which bundles SLED and SMASH, enables straightforward graphic integration from entry to waveforms. With a single click, cross-probing will display the waveforms in SMASH corresponding to the nets or devices currently selected in the schematics and operating points can be back-annotated into the schematics.

Design of multi-domain systems

SLED offers the capability to create highly flexible and complex models through graphic composition. It covers the modeling of any domain like analog electronics, digital electronics, mechanics, magnetic, thermal effects.

SLED is predestinated for multi-domain systems where designers are guided during wiring of symbols with intelligent type checking of terminals. And initializing homogeneous simulation of such heterogenic systems in SMASH avoids simulator couplings with its disadvantages in configuration, set up, convergence problems…
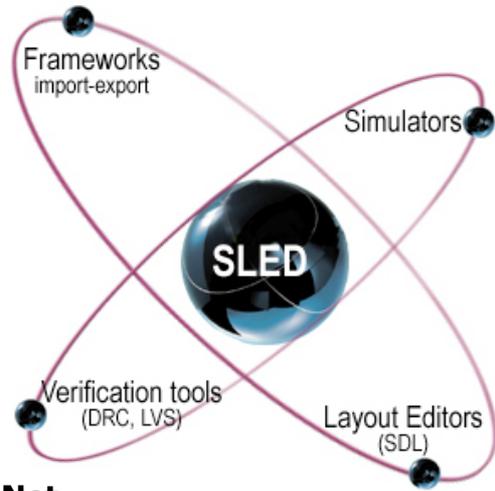
SledNet

SledNet provides mixed-signal and multi-language netlisting in SPICE, Verilog-HDL, VHDL & VHDL-AMS, including batch mode execution for automated non-regression testing.

Interoperability & compatibility

✓ Import of whole libraries and designs

From any release of the legacy ECS™ stem including Synario™, Cohesion Systems™, Laker AMS™…

✓ ASCII storage format

Storage of design data, including design or reference library configuration files, symbols, schematics… in ASCII format enables a script based approach for automatic symbol generation, library conversion, design library setup…

✓ Compatibility with other tools in the design chain

Built-in handling of Design Context configurations for multi-flavor SPICE netlisting (SMASH, Hspice, SDL, LVS…).

✓ EDIF Import/Export

Import/Export to and from EDIF provides the means to exchange full schematics, including graphics, with other design entry solutions, as well as to transfer designs to the next step in your Design Chain, such as Schematic Driven Layout (SDL).

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