SignalStorm® offers a unified signal integrity solution for cell-based design that accounts for propagation delay, IR drop, and crosstalk effects. It addresses next-generation, hierarchical delay calculation to provide the industry's most advanced technology for the signal integrity timing issues that are your critical concern for aggressive 0.18 micron designs and mainstream 0.13 micron designs.

**Figure 1: The average number of timing iterations is increasing due to deep submicron signal integrity issues**

### Benefits and Features

- Unified signal integrity solution for cell-based designs that accounts for both crosstalk and voltage (IR) drop in delay calculation
- The most accurate delay calculation for popular timing flows:
  - Unique time-quantized calculation of $C_{eff}$
  - Accurate multi-driven net and mesh handling
  - Non-linear modeling of instance-specific IR drop
  - Includes crosstalk-induced signal delays
- Fully hierarchical delay calculation provides fastest, most efficient commercial delay calculation with capacity for large, complex designs
  - 4x to 20x faster delay calculation
  - 80% less memory consumption
  - Identifies glitch transitions induced by crosstalk
- Production-proven technology
  - Includes advanced extraction technology
  - Leverages instance-specific IR drop data from VoltageStorm®
  - Used in dozens of high-performance, high-volume designs
- Optional, advanced driver model for aggressive, complex design styles
  - First commercial application of effective current source modeling (ECSM)
  - More accurately represents complex topologies
- Advanced, automatic library characterization
  - Automatic function recognition
  - .lib and ECSM characterization
  - Automatic SPICE job management
  - Binary search-based timing-check characterization
- Compatible with industry-standard libraries and popular static timing analysis tools
As process geometries continue to shrink, ever-thinner wires are packed more tightly together, producing unintended electrical effects, such as capacitance coupling and IR drop, which impair signal integrity. These complex signal integrity effects have a profound effect on path delays and design timing. As design starts move to 0.13 micron and below, signal integrity timing issues have become a primary concern, as they impede timing convergence, consume engineering resources and result in needless over-engineering, overly constrained designs and costly schedule delays (see Figure 1).

Current generation delay calculators don’t account for these complex signal integrity effects, so until now, you have been forced to increase your timing margins to allow for inaccuracies in delay calculation. But this is costly, since increasing a timing margin by as little as 5% can result in thousands of additional “failed” paths that you must resolve.

SignalStorm enables you to determine the impact of signal integrity effects on path delays with greater accuracy and speed than ever before. As a result, SignalStorm enables you to achieve timing convergence more quickly, conserving valuable engineering resources and speeding time-to-market.

**SUPERIOR ACCURACY, SPEED, AND CAPACITY**

SignalStorm incorporates several industry-first technologies to provide the most accurate delay calculation solution available today for the most popular timing analysis flows using the standard Liberty .lib format. Increased SignalStorm accuracy yields fewer false timing violations, conserving valuable engineering resources, speeding time-to-market and enabling more aggressive designs.

First, SignalStorm employs a time-quantized calculation of the effective load capacitance of receiver gates. This unique technology computes the effective capacitance over several time steps during the signal ramp to more closely track the actual effective capacitance as it changes with signal voltage.

SignalStorm also incorporates instance-based IR-drop data from VoltageStorm, to account for the effects of IR drop on path delays. This capability becomes critical at 0.13 micron and below, where power supplies are typically in the 1.2 volt range, and even small voltage drops can compromise signal timing and lead to chip failures. Unlike other delay calculators that treat IR drop as a simple voltage de-rating factor, SignalStorm models IR drop as a non-linear effect, avoiding the limited accuracy inherent in linear K-factors.

SignalStorm represents multi-driven nets and meshes with great accuracy, supporting complex clock distributions. Finally, SignalStorm accounts for the effects of cross-coupling between simultaneously transitioning signals with corrections to both delay calculations. Using the “glitch report” produced by SignalStorm, you can also analyze unintended transitions due to cross-couplings.

SignalStorm delay calculation is not only the most accurate available, it is also the fastest. An efficient, hierarchical database structure enables delay calculation that is 4 to 20 times faster while using only one-fifth the memory of other tools. A hierarchical database ensures any changes in child cells are automatically reflected in their parents. This unique, hierarchical data model enables SignalStorm to easily handle today’s largest, most complex SoC designs—without the need for you to build timing model extracts.

**DESIGN FLOW INTEGRATION**

SignalStorm integrates easily into standard timing verification flows. It can read library and design information from standard LEF/DEF and .lib formats using leading 3-D accurate extraction technology, which is embedded into SignalStorm, thus providing the best-possible parasitics for delay calculation. SignalStorm transfers the extracted RC data in binary format into the fully hierarchical database of the delay calculator, significantly reducing the amount of time needed for processing the RC files, and resulting in disk-space savings of more than 80%.

Alternatively, SignalStorm can read standard DSPF and SPEF files produced by other extraction processes. SignalStorm accepts instance-based IR drop data from VoltageStorm to account for the impact of IR drop on path delays.

SignalStorm outputs SDF files for use by industry-standard static timing analysis tools, and also produces text-based reports highlighting signal integrity risks.

**ECSM TIMING MODELS**

SignalStorm achieves breakthrough performance using industry-standard libraries in .lib format. For aggressive design styles that push process technologies to the edge, SignalStorm also offers an optional next-generation, advanced timing model format known as effective current source model (ECSM). ECSM format libraries model a cell’s non-linear output behavior as a current source, which more closely predicts actual silicon performance, particularly for complex nets.

SignalStorm is the first commercial tool to incorporate ECSM technology. Using ECSM libraries, SignalStorm accuracy is enhanced to within 2% of SPICE.
LIBRARY CHARACTERIZATION

SignalStorm library characterization technology speeds the production of high-quality libraries through a series of automated steps that can overcome the bottleneck of running SPICE. These steps include automatic function recognition, which minimizes the manual creation of the stimulus vectors for HSPICE. Automatic SPICE job management enables maximum utilization of SPICE resources with minimum effort. And binary search-based timing-check characterization minimizes the number of SPICE runs necessary to achieve accurate results.

Library characterization generates highly accurate .lib files as well as an ECSM database that provides more comprehensive data for precision delay calculation — especially important for complex network topologies. The ECSM database enables the delay calculator to utilize detailed driver current-voltage characteristics, rather than relying on reverse-engineered driver output waveforms from the delay and slew tables.

PRODUCTION PROVEN

SignalStorm, while new to the commercial marketplace, is a production-proven technology, already used in dozens of commercial designs. For example, SoC Design Foundry® has successfully completed 19 production designs using the SignalStorm technology, including some of the largest, most advanced, highest-volume designs in the market today. Because SignalStorm is based on specifications and feedback from SoC Design Foundry engineers, it addresses the most pressing needs for today’s leading-edge designs.

PLATFORM SUPPORT

SignalStorm runs on standard UNIX workstations from Sun Microsystems and Hewlett-Packard.

OS SUPPORT

- HP-UX 11
- Solaris 7 and Solaris 8

SYSTEM REQUIREMENTS

The system requirements will vary depending on your circuit size. However, here are some general guidelines:

MINIMUM CONFIGURATION

- DRAM 500 Mbytes
- Swap space 500 Mbytes

FOR MORE INFORMATION

Email us at info@cadence.com or log on to www.cadence.com

Figure 2: Signal integrity-aware delay calculation has been the missing link in timing analysis. SignalStorm takes into account timing and noise effects of crosstalk and IR drop; crucial for advanced deep-submicron designs.