Release	Description
INCISIVE 15.2	Incisive Formal Verifier
INCISIVE 15.2	Incisive Functional Safety Simulator
INCISIVE 15.2	Verifault(R)-XL simulator
INCISIVE 15.2	Incisive Enterprise Simulator - XL
INCISIVE 15.2	Digital Mixed Signal Option to IES
INCISIVE 15.2	Incisive Advanced Option
INCISIVE 15.2	Incisive Low-Power Simulation Option
INCISIVE 15.2	Incisive Advanced HAL Option
INCISIVE 15.2	AMS Designer with Flexible Analog Simulation
INCISIVE 15.2	Virtuoso AMS Designer Verification Option
INCISIVE 15.2	Incisive Enterprise Verifier - XL
INCISIVE 15.2	Incisive Coverage Unreachability App
INCISIVE 15.2	vManager Linux Client (Quantity 1)
INCISIVE 15.2	vManager Project Server
INDAGO 17.04	Indago Debug Analyzer App
SIGRITY 2017	Allegro Sigrity SI Base
SIGRITY 2017	Allegro Sigrity PI Base
SIGRITY 2017	Allegro Sigrity Power Aware SI Option
SIGRITY 2017	Allegro Sigrity Power Integrity Signoff and Optimization Option
SIGRITY 2017	Allegro Sigrity System Serial Link Option
SIGRITY 2017	Allegro Sigrity Package Assessment and Extraction Option
SPB 17.2	Cadence(R) SKILL Development Environment
SPB 17.2	Allegro Design Authoring High-Speed Option
SPB 17.2	Allegro Design Authoring Multi-Style Option
SPB 17.2	Allegro(R) Design Authoring Team Design Option
SPB 17.2	Allegro PCB Designer
SPB 17.2	Allegro PCB High-Speed Option
SPB 17.2	Allegro PCB Miniaturization Option
SPB 17.2	Allegro(R) PCB Symphony Team Design Option
SPB 17.2	Allegro(R) PCB Team Design Option
SPB 17.2	Allegro(R) PCB Analog/RF Option
SPB 17.2	Allegro PCB Design Planning Option

SPB 17.2	Allegro PCB Global Route Environment Option - XL
SPB 17.2	Cadence 3D Design Viewer
SPB 17.2	Allegro(R) ASIC Prototyping with FPGA's
SPB 17.2	Allegro PSpice(R) Simulator
SPB 17.2	Allegro PCB Routing Option
SPB 17.2	Allegro(R) PCB Librarian
SPB 17.2	Allegro(R) Physical Viewer
SPB 17.2	Cadence SiP Layout - XL
VIPCAT 11.3	Memory Model Portfolio
VIPCAT 11.3	VIP for MR-IOV
VIPCAT 11.3	VIP for OCP 3.0
VIPCAT 11.3	PureView
VIPCAT 11.3	SOC Portfolio
XCELIUM 17.04	Cadence(R) Simulation Analysis Environment (SimVision)
XCELIUM 17.04	Xcelium Single-Core
XCELIUM 17.04	Xcelium Digital Mixed Signal Option

Release	Description
CONFRML 17.1	Conformal Constraint Designer - XL
CONFRML 17.1	CCD Multi-Constraint Check Option
CONFRML 17.1	Conformal Low Power - GXL
CONFRML 17.1	Conformal ECO Designer - GXL
EXT 17.1	Cadence Quantus QRC Extraction - XL
EXT 17.1	Cadence Quantus QRC Advanced Analysis GXL Option
EXT 17.1	Cadence Quantus QRC Advanced Modeling GXL Option
EXT 17.1	Cadence Quantus QRC Display Technology Option
EXT 17.1	Cadence Quantus QRC Advanced Modeling20 GXL Option
GENUS 17.1	Genus Synthesis Solution
GENUS 17.1	Genus Low Power Option
GENUS 17.1	Genus Physical Option
GENUS 17.1	Genus CPU Accelerator Option
INDAGO 17.04	Indago Debug Analyzer App
LIBERATE 16.1	Virtuoso Liberate Server
LIBERATE 16.1	Virtuoso Liberate Client
LIBERATE 16.1	Virtuoso Liberate LV Server
LIBERATE 16.1	Virtuoso Liberate LV Client
MDV 17.04	vManager Linux Client (Quantity 1)
MDV 17.04	vManager Project Server
MODUS 17.1	Modus ATPG
MODUS 17.1	Modus DFT Option
MODUS 17.1	Modus Hierarchical Option
MVS 17.1	Virtuoso LDE Analyzer Option
MVS 17.1	Innovus DFM Option
SPECTRE 16.1	Spectre(R) RelXpert Reliability Simulator
SPECTRE 16.1	Spectre Multi-mode Simulation
SPECTRE 16.1	Spectre Multi-mode Simulation
SPECTRE 16.1	Spectre(R) CPU Accelerator Option
SPECTRE 16.1	Spectre Extensive Partitioned Simulator
SSV 17.1	Tempus Timing Signoff Solution XL
SSV 17.1	Tempus Timing Signoff Solution ECO

SSV 17.1	Tempus Timing Signoff Solution MP
SSV 17.1	Voltus IC Power Integrity Solution - XL (VTS-XL)
SSV 17.1	Voltus IC Power Integrity Solution Advanced Analysis GXL Option (VTS-AA)
SSV 17.1	Voltus IC Power Integrity Solution - MP (VTS-MP) (Acceleration Option to Voltus IC XL (VTS200))
IC 6.1.7	Cadence(R) Design Framework II
IC 6.1.7	Cadence Framework Integration Runtime Option
IC 6.1.7	Cadence(R) Design Framework Integrator's Toolkit
IC 6.1.7	Virtuoso(R) Simulation Environment
IC 6.1.7	Virtuoso(R) Schematic VHDL Interface
IC 6.1.7	Virtuoso(R) Schematic Editor Verilog(R) Interface
IC 6.1.7	Virtuoso(R) Schematic Editor HSPICE Interface
IC 6.1.7	Virtuoso(R) Analog Oasis Run-Time Option
IC 6.1.7	Cadence(R) OASIS for RFDE
IC 6.1.7	Virtuoso(R) Analog HSPICE Interface Option
IC 6.1.7	Virtuoso(R) AMS Designer Environment
IC 6.1.7	Dracula(R) Design Rule Checker
IC 6.1.7	Dracula(R) Layout Vs. Schematic Verifier
IC 6.1.7	Dracula(R) Parasitic Extractor
IC 6.1.7	Diva(R) Design Rule Checker
IC 6.1.7	Diva(R) Layout Vs. Schematic Verifier
IC 6.1.7	Diva(R) Parasitic Extractor
IC 6.1.7	Cadence(R) SKILL Development Environment
IC 6.1.7	Virtuoso(R) EDIF 200 Reader
IC 6.1.7	Virtuoso(R) EDIF 200 Writer
IC 6.1.7	Virtuoso(R) Schematic Editor XL
IC 6.1.7	Virtuoso(R) Analog Design Environment - GXL
IC 6.1.7	Virtuoso(R) Visualization & Analysis XL
IC 6.1.7	Virtuoso(R) ADE Assembler
IC 6.1.7	Virtuoso(R) Variation Option
IC 6.1.7	Virtuoso(R) ADE Verifier
IC 6.1.7	Virtuoso(R) DFM Option
IC 6.1.7	Virtuoso(R) Layout Suite - GXL
IC 6.1.7	Virtuoso Layout Suite GXL

IC 6.1.7	Virtuoso Implementation Aware Design Option
IC 6.1.7	Virtuoso Layout Suite EAD
IC 6.1.7	Virtuoso EAD 3D Precision Solver
IC 6.1.7	Virtuoso EAD Advanced Electrical Analysis
IC 6.1.7	Voltus-Fi Custom Power Integrity Solution - XL
PVS 16.1	Cadence(R) Physical Verification System Design Rule Checker XL
PVS 16.1	Cadence(R) Physical Verification System Layout vs. Schematic Checker XL
PVS 16.1	Cadence(R) Physical Verification System Programmable Electrical Rules Checker
PVS 16.1	Cadence(R) Physical Verification System Design Analysis Option
PVS 16.1	Cadence(R) Physical Verification System Constraint Validator
PVS 16.1	Cadence Physical Verification System Constraint Validator XL
PVS 16.1	Cadence Physical Verification System Advanced Analysis Option for PVS DRC XL (96210)
PVS 16.1	Cadence(R) Physical Verification System Advanced Device Option
PVS 16.1	Virtuoso(R) Integrated Physical Verification System Option for Virtuoso Layout Suite (95300, 95310)
PVS 16.1	Cadence(R) QuickView Layout and Mask Data Viewer
PVS 16.1	Cadence QuickView Sign-Off Data Analysis Environment
VIPCAT 11.3	Memory Model Portfolio
VIPCAT 11.3	VIP for MR-IOV
VIPCAT 11.3	VIP for OCP 3.0
VIPCAT 11.3	PureView
VIPCAT 11.3	SOC Portfolio
JLS 17.1	Joules RTL Power Solution
XCELIUM 17.04	Cadence(R) Simulation Analysis Environment (SimVision)
XCELIUM 17.04	Xcelium Single-Core
XCELIUM 17.04	Xcelium Digital Mixed Signal Option
INCISIVE 15.2	Incisive Formal Verifier
INCISIVE 15.2	Incisive Functional Safety Simulator
INCISIVE 15.2	Verifault(R)-XL simulator
INCISIVE 15.2	Incisive Enterprise Simulator - XL
INCISIVE 15.2	Digital Mixed Signal Option to IES
INCISIVE 15.2	Incisive Advanced Option
INCISIVE 15.2	Incisive Low-Power Simulation Option
INCISIVE 15.2	Incisive Advanced HAL Option

INCISIVE 15.2	AMS Designer with Flexible Analog Simulation
INCISIVE 15.2	Virtuoso AMS Designer Verification Option
INCISIVE 15.2	Incisive Enterprise Verifier - XL
INCISIVE 15.2	Incisive Coverage Unreachability App
INCISIVE 15.2	vManager Linux Client (Quantity 1)
INCISIVE 15.2	vManager Project Server
INNOVUS 17.1	Innovus Implementation System
INNOVUS 17.1	Innovus 20/16/14nm Option
INNOVUS 17.1	Innovus Mixed Signal Option
INNOVUS 17.1	Innovus High Frequency Route Option
INNOVUS 17.1	Innovus Hierarchical Design Option
INNOVUS 17.1	Innovus CPU Accelerator Option

Release	Description
SIGRITY 2017	Allegro Sigrity SI Base
SPB 17.2	Allegro PCB Designer
SPB 17.2	Allegro(R) AMS Simulator
SPB 17.2	Allegro 2 FPGA System Planner Option

Release	Description
VIPCAT 11.3	Memory Model Portfolio
VIPCAT 11.3	VIP for MR-IOV
VIPCAT 11.3	VIP for OCP 3.0
VIPCAT 11.3	PureView
VIPCAT 11.3	SOC Portfolio
CONFRML 17.1	Conformal Constraint Designer - XL
CONFRML 17.1	CCD Multi-Constraint Check Option
CONFRML 17.1	Conformal Low Power - GXL
GENUS 17.1	Genus Synthesis Solution
GENUS 17.1	Genus Low Power Option
GENUS 17.1	Genus CPU Accelerator Option
INDAGO 17.04	Indago Debug Analyzer App
INCISIVE 15.2	Incisive Functional Safety Simulator
INCISIVE 15.2	Incisive Coverage Unreachability App
INCISIVE 15.2	Incisive Advanced HAL Option
INCISIVE 15.2	Incisive Advanced Option
INCISIVE 15.2	Incisive Formal Verifier
INCISIVE 15.2	Incisive Low-Power Simulation Option
INCISIVE 15.2	AMS Designer with Flexible Analog Simulation
INCISIVE 15.2	Virtuoso AMS Designer Verification Option
INCISIVE 15.2	Digital Mixed Signal Option to IES
INCISIVE 15.2	Incisive Enterprise Simulator - XL
INCISIVE 15.2	Incisive Enterprise Verifier - XL
INCISIVE 15.2	Verifault(R)-XL simulator
INCISIVE 15.2	vManager Project Server
INCISIVE 15.2	vManager Linux Client (Quantity 1)
XCELIUM 17.04	Cadence(R) Simulation Analysis Environment (SimVision)
XCELIUM 17.04	Xcelium Single-Core
XCELIUM 17.04	Xcelium Digital Mixed Signal Option

Virtuoso Advanced Node Option to the IC Package

Release	Description
EXT 17.1	Cadence Quantus QRC Advanced Node Modeling Option
ICADV 12.3	Virtuoso Advanced Node Framework
ICADV 12.3	Virtuoso Advanced Node Option for Layout
ICADV 12.3	Virtuoso Advanced Node Option for Layout Standard
MVS 17.1	Litho Electrical Analyzer
MVS 17.1	Litho Physical Analyzer
MVS 17.1	Distributed Process for 8 CPUs
MVS 17.1	Cadence Litho Hotspot Fixing Option
PVS 16.1	Virtuoso Integrated Physical Verification System Advanced Analysis Option for IPVS (96400)

JasperGold Formal Verification Option to the IC Package

Release	Description
JASPER 17.06	JasperGold Automatic Formal Linting App
JASPER 17.06	JasperGold Connectivity Verification APP
JASPER 17.06	JasperGold Coverage APP Option
JASPER 17.06	JasperGold Formal Property Verification APP
JASPER 17.06	JasperGold Interactive Option
JASPER 17.06	JasperGold Structural Property Synthesis APP
JASPER 17.06	JasperGold X-Propagation Verification APP
JASPER 17.06	JasperGold Behavioral Property Synthesis APP
JASPER 17.06	JasperGold CDC Verification App
JASPER 17.06	JasperGold CSR Verification APP
JASPER 17.06	JasperGold Low Power Verification APP
JASPER 17.06	JasperGold Sequential Equivalency Checking APP
JASPER 17.06	JasperGold Security Path Verification APP

Stratus High Level Synthesis Option to the IC or TLM packages

Release	Description
STRATUS 17.1	Stratus HLS - XL
STRATUS 17.1	Stratus Floating Point

Virtuoso Liberate AMS Mixed Signal Characterisation Option to the IC Package

Release	Description
LIBERATE 16.1	Virtuoso Variety Server
LIBERATE 16.1	Virtuoso Variety Client
LIBERATE 16.1	Virtuoso Liberate MX Server
LIBERATE 16.1	Virtuoso Liberate MX Client
LIBERATE 16.1	Virtuoso Liberate AMS Server
LIBERATE 16.1	Virtuoso Liberate AMS Client

3D-IC Option to the IC Package

Release	Description
INNOVUS 17.1	Innovus 3D-IC Option

System in Package (SiP) Option to he IC and Systems packages

Release	Description
IC 6.1.7	Virtuoso System Design Platform
SIGRITY 2017	Cadence IO-SSO Analysis Suite
SIGRITY 2017	Voltus IC Power Integrity Solution - Sigrity Package Analysis (VTS-SPA) (Package Analysis Option to Voltus-AA)
SIGRITY 2017	PowerSI 3D EM Full-Wave Extraction Option
SPB 17.2	Allegro Relational Rules Developer
SPB 17.2	Allegro Relational Rules Checker
SPB17.2	Orbit IO