Release	Description
SIGRITY 2016	Allegro Sigrity Power Aware SI Option
SIGRITY 2016	Allegro Sigrity System Serial Link Option
SIGRITY 2016	Allegro Sigrity Package Assessment and Extraction Option
SIGRITY 2016	Allegro Sigrity SI Base
SIGRITY 2016	Allegro Sigrity Power Integrity Signoff and Optimization Option
SIGRITY 2016	Allegro Sigrity PI Base
SPB 17.2	Allegro PCB Designer
SPB 17.2	Allegro PCB High-Speed Option
SPB 17.2	Allegro PCB Miniaturization Option
SPB 17.2	Allegro(R) PCB Team Design Option
SPB 17.2	Allegro PCB Routing Option
SPB 17.2	Allegro PCB Design Planning Option
SPB 17.2	Allegro(R) PCB Librarian
SPB 17.2	Allegro(R) ASIC Prototyping with FPGA's
SPB 17.2	Allegro Design Authoring Multi-Style Option
SPB 17.2	Allegro(R) AMS Simulator
SPB 17.2	Allegro(R) PCB Analog/RF Option
SPB 17.2	Cadence SiP Layout - XL
SPB 17.2	Cadence 3D Design Viewer
SPB 17.2	Allegro(R) Design Authoring Team Design Option
SPB 17.2	Allegro(R) Physical Viewer
SPB 17.2	Allegro Design Authoring High-Speed Option
SPB 17.2	Allegro PCB Global Route Environment Option - XL
SPB 17.2	Cadence(R) SKILL Development Environment
INCISIVE 15.2	Incisive Functional Safety Simulator
INCISIVE 15.2	Incisive Coverage Unreachability App
INCISIVE 15.2	Incisive Advanced HAL Option
INCISIVE 15.2	Incisive Advanced Option
INCISIVE 15.2	Incisive Formal Verifier
INCISIVE 15.2	Incisive Low-Power Simulation Option
INCISIVE 15.2	AMS Designer with Flexible Analog Simulation
INCISIVE 15.2	Virtuoso AMS Designer Verification Option

INCISIVE 15.2	Digital Mixed Signal Option to IES
INCISIVE 15.2	Incisive Enterprise Simulator - XL
INCISIVE 15.2	Incisive Enterprise Verifier - XL
INCISIVE 15.2	Verifault(R)-XL simulator
INCISIVE 15.2	vManager Project Server
INCISIVE 15.2	vManager Linux Client (Quantity 1)
INDAGO 15.2	Indago Debug Analyzer App
VIPCAT 11.3	Memory Model Portfolio
VIPCAT 11.3	VIP for MR-IOV
VIPCAT 11.3	VIP for OCP 3.0
VIPCAT 11.3	SOC Portfolio
VIPCAT 11.3	PureView

Release	Description
CONFRML 16.1	CCD Multi-Constraint Check Option
CONFRML 16.1	Encounter (R) Conformal Constraint Designer - XL
CONFRML 16.1	Encounter Conformal Low Power - GXL
CONFRML 16.1	Encounter Conformal ECO Designer - GXL
EDI 14.2	Encounter Digital Implementation System XL
EDI 14.2	Encounter CPU Accelerator Option
EDI 14.2	Encounter Low Power GXL Option
EDI 14.2	Encounter Mixed Signal GXL Option
EDI 14.2	Encounter Giga Scale GXL Option
EDI 14.2	Encounter Universal 20 GXL Option
EDI 14.2	Encounter Clock Concurrent Optimization
EDI 14.2	Encounter Advanced Node GXL Option
ET 15.1	Encounter True Time ATPG Advanced
ET 15.1	Option to RC - DFT Architect Advanced
ET 15.1	Encounter Test LBIST Option
ET 15.1	Encounter Test Advanced MBIST Option
ET 15.1	Encounter Diagnostics Basic
EXT 15.2	Cadence QRC Advanced Modeling20 GXL Option
EXT 15.2	Cadence QRC Extraction - XL
EXT 15.2	Cadence QRC Advanced Modeling GXL Option
EXT 15.2	Cadence QRC Advanced Analysis GXL Option
EXT 15.2	Cadence QRCX Display Technology Option
GENUS 16.1	Genus Synthesis Solution
GENUS 16.1	Genus Low Power Option
GENUS 16.1	Genus Physical Option
GENUS 16.1	Genus CPU Accelerator Option
IC 6.1.7	Virtuoso(R) Layout Suite - GXL
IC 6.1.7	Virtuoso(R) Analog Design Environment - GXL
IC 6.1.7	Virtuoso Implementation Aware Design Option
IC 6.1.7	Virtuoso EAD Advanced Electrical Analysis
IC 6.1.7	Virtuoso Layout Suite EAD
IC 6.1.7	Cadence(R) SKILL Development Environment

IC 6.1.7	Virtuoso(R) Layout Suite - GXL
IC 6.1.7	Virtuoso(R) EDIF 200 Reader
IC 6.1.7	Virtuoso(R) Layout Suite - GXL
IC 6.1.7	Virtuoso(R) Schematic Editor XL
IC 6.1.7	Virtuoso(R) Visualization & Analysis XL
IC 6.1.7	Dracula(R) Design Rule Checker
IC 6.1.7	Virtuoso(R) DFM Option
IC 6.1.7	Virtuoso(R) Analog Oasis Run-Time Option
IC 6.1.7	Diva(R) Layout Vs. Schematic Verifier
IC 6.1.7	Diva(R) Design Rule Checker
IC 6.1.7	Dracula(R) Parasitic Extractor
IC 6.1.7	Diva(R) Parasitic Extractor
IC 6.1.7	Virtuoso(R) Schematic VHDL Interface
IC 6.1.7	Virtuoso(R) Schematic Editor Verilog(R) Interface
IC 6.1.7	Virtuoso(R) EDIF 200 Writer
IC 6.1.7	Virtuoso(R) AMS Designer Environment
IC 6.1.7	Cadence(R) Design Framework II
IC 6.1.7	Cadence(R) OASIS for RFDE
IC 6.1.7	Virtuoso(R) Schematic Editor HSPICE Interface
IC 6.1.7	Dracula(R) Layout Vs. Schematic Verifier
IC 6.1.7	Cadence Framework Integration Runtime Option
IC 6.1.7	Cadence(R) Design Framework Integrator's Toolkit
IC 6.1.7	Virtuoso(R) Simulation Environment
IC 6.1.7	Virtuoso(R) Analog HSPICE Interface Option
IC 6.1.7	Virtuoso(R) Layout Suite - GXL
IC 6.1.7	Virtuoso EAD 3D Precision Solver
IC 6.1.7	Virtuoso(R) ADE Assembler
IC 6.1.7	Virtuoso(R) Variation Option
IC 6.1.7	Virtuoso(R) ADE Verifier
IC 6.1.7	Virtuoso Layout Suite GXL
IC 6.1.7	Voltus-Fi Custom Power Integrity Solution - XL
INCISIVE 15.2	Incisive Functional Safety Simulator
INCISIVE 15.2	Incisive Coverage Unreachability App

INCISIVE 15.2	Incisive Advanced HAL Option
INCISIVE 15.2	Incisive Advanced Option
INCISIVE 15.2	Incisive Formal Verifier
INCISIVE 15.2	Incisive Low-Power Simulation Option
INCISIVE 15.2	AMS Designer with Flexible Analog Simulation
INCISIVE 15.2	Virtuoso AMS Designer Verification Option
INCISIVE 15.2	Digital Mixed Signal Option to IES
INCISIVE 15.2	Incisive Enterprise Simulator - XL
INCISIVE 15.2	Incisive Enterprise Verifier - XL
INCISIVE 15.2	Verifault(R)-XL simulator
INCISIVE 15.2	vManager Project Server
INCISIVE 15.2	vManager Linux Client (Quantity 1)
INDAGO 15.2	Indago Debug Analyzer App
INNOVUS 16.1	Innovus CPU Accelerator Option
INNOVUS 16.1	Innovus Mixed Signal Option
INNOVUS 16.1	Innovus Hierarchical Design Option
INNOVUS 16.1	Innovus Implementation System
INNOVUS 16.1	Innovus 20/16/14nm Option
INNOVUS 16.1	Innovus High Frequency Route Option
LIBERATE 15.1	Virtuoso Liberate Server
LIBERATE 15.1	Virtuoso Liberate Client
LIBERATE 15.1	Virtuoso Liberate LV Server
LIBERATE 15.1	Virtuoso Liberate LV Client
MMSIM 15.1	Spectre Extensive Partitioned Simulator
MMSIM 15.1	Virtuoso(R) RelXpert
MMSIM 15.1	Virtuoso Multi-mode Simulation with Spectre XPS
MMSIM 15.1	Virtuoso Multi-mode Simulation with Spectre XPS
MMSIM 15.1	Virtuoso Multi-mode Simulation CPU Accelerator option
MODUS 16.1	Modus Test
MODUS 16.1	Modus DFT Option
MODUS 16.1	Modus Hierarchical Option
MVS 16.1	Innovus DFM GXL Option
MVS 16.1	Encounter DFM GXL Option

MVS 16.1	Virtuoso LDE Analyzer Option
PVS 15.1	Cadence(R) Physical Verification System Programmable Electrical Rules Checker
PVS 15.1	PVS Design Analysis Option
PVS 15.1	PVS Design Analysis Option
PVS 15.1	Cadence(R) Physical Verification System Layout vs. Schematic Checker XL
PVS 15.1	Cadence(R) Physical Verification System Layout vs. Schematic Checker XL
PVS 15.1	Cadence(R) Physical Verification System Design Rule Checker XL
PVS 15.1	Cadence(R) Physical Verification System Design Rule Checker XL
PVS 15.1	Virtuoso(R) Integrated Physical Verification System Option for Virtuoso Layout Suite (95300, 95310)
PVS 15.1	Cadence Physical Verification System Advanced Analysis Option for PVS DRC XL (96210)
PVS 15.1	Cadence Physical Verification System Advanced Analysis Option for PVS DRC XL (96210)
PVS 15.1	Cadence(R) Physical Verification System Constraint Validator
PVS 15.1	Cadence(R) Physical Verification System Constraint Validator XL
PVS 15.1	Cadence(R) Physical Verification System Advanced Device Option
PVS 15.1	Cadence(R) QuickView Layout and Mask Data Viewer
PVS 15.1	Cadence QuickView Sign-Off Data Analysis Environment
RC 14.2	Encounter RTL Compiler - XL
RC 14.2	Encounter RTL Compiler CPU Accelerator Option
RC 14.2	Encounter RTL Compiler Low Power Option
RC 14.2	Encounter RTL Compiler Advanced Physical Option
SSV 16.1	Voltus IC Power Integrity Solution - XL (VTS-XL)
SSV 16.1	Tempus Timing Signoff Solution XL
SSV 16.1	Voltus IC Power Integrity Solution Advanced Analysis GXL Option (VTS-AA)
SSV 16.1	Tempus Timing Signoff Solution MP
SSV 16.1	Tempus Timing Signoff Solution TSO
SSV 16.1	Voltus IC Power Integrity Solution - MP (VTS-MP) (Acceleration Option to Voltus IC XL (VTS200))
VIPCAT 11.3	Memory Model Portfolio
VIPCAT 11.3	VIP for MR-IOV
VIPCAT 11.3	VIP for OCP 3.0
VIPCAT 11.3	SOC Portfolio
VIPCAT 11.3	PureView

Release	Description
SIGRITY 2016	Allegro Sigrity SI Base
SPB 17.2	Allegro PCB Designer
SPB 17.2	Allegro(R) AMS Simulator
SPB 17.2	Allegro 2 FPGA System Planner Option

Release	Description
INCISIVE 15.2	Cadence System Creator - L
INCISIVE 15.2	Embedded Software Debug App
INDAGO152	Indago Embedded Software Debug App
CONFRML 16.1	CCD Multi-Constraint Check Option
CONFRML 16.1	Encounter (R) Conformal Constraint Designer - XL
CONFRML 16.1	Encounter Conformal Low Power - GXL
GENUS 16.1	Genus Synthesis Solution
GENUS 16.1	Genus Low Power Option
GENUS 16.1	Genus CPU Accelerator Option
RC 14.2	Encounter RTL Compiler - XL
RC 14.2	Encounter RTL Compiler CPU Accelerator Option
RC 14.2	Encounter RTL Compiler Low Power Option
INCISIVE 15.2	Incisive Functional Safety Simulator
INCISIVE 15.2	Incisive Coverage Unreachability App
INCISIVE 15.2	Incisive Advanced HAL Option
INCISIVE 15.2	Incisive Advanced Option
INCISIVE 15.2	Incisive Formal Verifier
INCISIVE 15.2	Incisive Low-Power Simulation Option
INCISIVE 15.2	AMS Designer with Flexible Analog Simulation
INCISIVE 15.2	Virtuoso AMS Designer Verification Option
INCISIVE 15.2	Digital Mixed Signal Option to IES
INCISIVE 15.2	Incisive Enterprise Simulator - XL
INCISIVE 15.2	Incisive Enterprise Verifier - XL
INCISIVE 15.2	Verifault(R)-XL simulator
INCISIVE 15.2	vManager Project Server
INCISIVE 15.2	vManager Linux Client (Quantity 1)
INDAGO 15.2	Indago Debug Analyzer App
VIPCAT 11.3	Memory Model Portfolio
VIPCAT 11.3	VIP for MR-IOV
VIPCAT 11.3	VIP for OCP 3.0
VIPCAT 11.3	SOC Portfolio
VIPCAT 11.3	PureView

Virtuoso Advanced Node Option to the IC Package

Release	Description
EXT 15.2	Cadence Quantus QRC Advanced Node Modeling Option
ICADV 12.2	Virtuoso Advanced Node Framework
ICADV 12.2	Virtuoso Advanced Node Option for Layout
ICADV 12.2	Virtuoso Advanced Node Option for Layout Standard
MVS 16.1	Litho Physical Analyzer
MVS 16.1	Distributed Process for 8 CPUs
MVS 16.1	Litho Electrical Analyzer
MVS 16.1	Cadence Litho Hotspot Fixing Option
PVS 15.1	Virtuoso Integrated Physical Verification System Advanced Analysis Option for IPVS (96400)

JasperGold Formal Verification Option to the IC Package

Release	Description
JASPER 16.06	JasperGold Interactive Option
JASPER 16.06	JasperGold Formal Property Verification APP
JASPER 16.06	JasperGold X-Propagation Verification APP
JASPER 16.06	JasperGold Connectivity Verification APP
JASPER 16.06	JasperGold Structural Property Synthesis APP
JASPER 16.06	JasperGold Coverage APP Option
JASPER 16.06	JasperGold Automatic Formal Linting App

Stratus High Level Synthesis Option to the IC or TLM packages

Release	Description
STRATUS 16.1	Stratus HLS - XL
STRATUS 16.1	Stratus Floating Point

Virtuoso Liberate AMS Mixed Signal Characterisation Option to the IC Package

Release	Description
LIBERATE 15.1	Virtuoso Liberate AMS Server
LIBERATE 15.1	Virtuoso Liberate AMS Client

3D-IC Option to the IC Package

Release	Description
IC 6.1.7	Virtuoso Stacked Die Option
EDI 14.2	Encounter Stacked Die GXL Option
INNOVUS 16.1	Innovus 3D-IC Option

System in Package (SiP) Option to he IC and Systems packages

Release	Description
SIGRITY 2016	Voltus IC Power Integrity Solution - Sigrity Package Analysis (VTS-SPA) (Package Analysis Option to Voltus-AA)
SIGRITY 2016	Cadence IO-SSO Analysis Suite