EUROPRACTICE
TRAINING COURSES

Advanced design flow training courses for the support of student training and research in the European academic sector

2019

Training Courses

EUROPRACTICE

EUROPRACTICE training courses use a combination of lectures and practical sessions to explain specific design flows. The courses are developed to enable delegates to better understand the challenges of successful design by appropriate use of design tools and design methodologies.

EUROPRACTICE training courses are open to Professors, Lecturers, Academic Staff and Postgraduate Students from established academic sites who are either Academic or Research Laboratory members of EUROPRACTICE.

EUROPRACTICE training courses are provided by expert staff from the EUROPRACTICE partners and will be held at the partner's dedicated training facilities in Cork (Ireland), Didcot (UK), Erlangen (Germany), Grenoble (France) and Leuven (Belgium). Booking and administration of EUROPRACTICE training courses is provided by STFC Rutherford Appleton Laboratory on behalf of the EUROPRACTICE partners irrespective of the training course location.

EUROPRACTICE training courses use realistic design examples and most courses include practical sessions that will use technologies available through Europractice, for example design tools that are available to members through the EUROPRACTICE design tool service and technologies available from the EUROPRACTICE IC service.

Further details of the EUROPRACTICE training courses can be found within this booklet. For the latest course schedule and online booking please visit the website:

www.europractice.stfc.ac.uk/training

Course Highlights include:

This project has received funding from the European Union's H2020 programme for research, technological development and demonstration under grant agreement 825121

EUROPRACTICE
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Comprehensive Digital IC Implementation and Sign-Off

This course takes participants through a full state of the art Digital IC implementation flow, covering the design flows and tools required to successfully implement modern Digital IC designs, ready for manufacture. The course starts with known good RTL code, and examines; synthesis (low power, test and physical), timing constraints, physical implementation (floorplanning, placement, CTS and Routing), design finishing, and signoff checks.

Theory and concepts are covered in lectures with significant time given to detailed hands-on practical exercises. The design flow is illustrated with an RTL SoC example which is then taken through to layout (GDSII suitable for manufacture) in a 65nm CMOS process.

Course schedule:

Day 1
- Introduction and Digital Design Flows
- IC Implementation Fundamentals
- Starting with Synthesis
- SDC Timing Constraints
- Mapping, Optimisation & Design Analysis

Day 2
- Low Power Optimisation
- Scan Test Synthesis
- Physical Synthesis

Day 3
- Place and Route flow
- MCMM Timing analysis, OCV and constraints setup
- Design Import
- Floorplanning & Powerplanning
- Early DRC

Day 4
- Placement
- Clock Tree Synthesis
- Routing and Design Finishing
- Verification
- Data Export
- Signoff DRC

Day 5
- Formal Equivalence Checking and Debug
- Signoff Static timing analysis with SI analysis
- Gate level simulation
- Signoff Power Analysis
- Automatic Test Pattern Generation

The course is aimed at digital circuit designers who are either new to digital IC design or who wish to update their previous knowledge to the latest design flows and tool methodologies required to implement standard cell (semi-custom) digital ICs with a modern process. The actual development of the design's RTL code is outside of the scope of this course.

Comprehensive Digital IC Implementation and Sign-Off
offered using either a Cadence or Synopsys design tool flow and a UMC 65nm process

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

Presented by STFC staff

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

Only pre-booked and confirmed delegates may attend. Attendance is also subject to payment of course fees and signature of appropriate technology non-disclosure agreements and tool license agreements.

For further details, course dates and online booking:

www.europractice.stfc.ac.uk

Advanced Low Power Digital IC Implementation

This course focuses on the advanced low power digital implementation techniques which are used to minimise power (both dynamic and leakage) in modern digital ICs.

The course covers a comprehensive range of low power techniques using UPF, including: Clock gating, use of Multi-VTH and Multi-channel libraries, Multi-Voltage, Power gating (MTCMOS), and Dynamic Voltage and Frequency Scaling (DVFS).

Theory and concepts are explained in the lectures and are illustrated with extensive hands-on practical exercises using an SoC design example which is taken from RTL through to layout in a 40nm GlobalFoundries technology.

By the end of the course, you should be able to:
- Run early analyses to identify power reduction opportunities
- Create a UPF file for a design
- Implement advanced low power techniques
- Dynamically and statically verify a design with UPF

Course schedule:

Day 1
- Introduction and Design Flows
- Standard Cell Library Choices
  - Library analysis
- Low Power Design Strategies
- Power Analysis and Switching Activity Information
  - Power estimation and exploration

Day 2
- Low Power Constraints Specification using UPF
  - UPF Creation and Checking
- Low Power Verification
  - RTL Simulation with UPF
- Low Power RTL Synthesis
  - Synthesis: Power gating and static multi-voltage

Day 3
- Low Power Physical Implementation
  - Physical Implementation: Power gating and static multi-voltage
  - Low Power Verification with UPF
  - Gate level simulation with UPF
- Dynamic Multi-Voltage Implementation
  - UPF creation & Synthesis for Dynamic Multi-Voltage
  - Dynamic Multi-Voltage Physical Implementation
  - Verification of Dynamic Multi-Voltage

Prerequisites: The course is aimed at digital IC designers who are already familiar with digital IC design using standard cell design flows. Existing understanding of the basic Digital IC design flow is required, or prior attendance of the EUROPRACTICE *"Comprehensive Digital IC Implementation & Signoff"* course.

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Advanced Low Power Digital IC Implementation
offered using either a Cadence or Synopsys design tool flow and a 40nm GlobalFoundries technology

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

Presented by STFC staff

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EUROPRACTICE
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Advanced digital physical implementation flow (featuring low power)

imec,
Kapeldreef 75, 3001 Leuven,
Belgium

Presented by imec staff

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

Only pre-booked and confirmed delegates may attend. Attendance is also subject to payment of course fees and signature of appropriate technology non-disclosure agreements and tool license agreements.

For further details, course dates and online booking:

www.europractice.stfc.ac.uk

Advanced digital physical implementation flow (featuring low power)

The participants will become familiar with the changes introduced in the IC design flows for advanced deep submicron technology nodes.

Are you interested in the changes introduced in the IC design flow for advanced deep submicron technology nodes? Are you searching for a deeper understanding of the low-power issues? Do you want to know everything about relevant process parameters and IP-libraries? Or do you want to become familiar with future design flow challenges? A hands-on course with experts who daily face the do's-and-don'ts in physical design will bring you to the next level. State-of-the-art EDA tools and relevant design exercises in the 65-40nm technology bring you to a more advanced level of implementation skill.

State-of-the-art EDA tools and relevant design exercises will bring the participants to a level at which they can confidently face future design flow challenges introduced by the 65 nm process characteristics and constraints.

Course schedule:

Day 1
- Introduction
- Power aware design
- Design planning
- Low power flow
- Lab session: CPF and logical synthesis

Day 2
- Library analysis and management
- IP integration and management
- Placement and optimization
- Clock tree synthesis
- Lab session: Floorplan and placement

Day 3
- Design For Test (DFT)
- MultiMode and MultiCorner (MMMC)
- Routing
- Lab session: Clock tree synthesis and route MMMC

Day 4
- IR drop analysis
- On-chip variation
- Sign-off
- Design finishing & layout verification
- Tape-out
- Lab session: Sign-off verification

Prerequisites: Course participants should be familiar with IC design and should have a basic understanding of the IC design flow

VHDL language and Design Flow

VHDL is a standard worldwide language for the design, documentation and description of electronic systems at the component, board or system level. It supports design verification through simulation and design creation through synthesis.

This 5-day course is centered on VHDL syntax (through example) while emphasizing good code style and the link to hardware. During the course the participants will:

- Be introduced to VHDL and the test-bench concepts
- Learn how to efficiently simulate VHDL models
- Be introduced to the VHDL synthesizable sub-set
- Learn that 'what you write is what you get', i.e. that the synthesized netlist is dependent on how the code is written
- Learn how to tackle issues like: sharing, asynchronous logic, initialization
- Get some experience with synthesis of the VHDL code into a gate level netlist using clock gating techniques to reduce the power
- Learn how to insert basic test logic and generate test patterns
- Be introduced to performing power analysis, generating test patterns and running logic equivalence checks

Course schedule:

Day 1: Introduction (using Modelsim for simulation)
- Flow overview: from specification to tested dies
- VHDL background, versions & basic concepts
- Entities, architectures, process, hierarchy

Day 2: VHDL for synthesis (using Synopsys Design Compiler)
- Packages, libraries, types, signals, variables
- Logic and memory inference
- High level optimizations (resource sharing etc.)

Day 3: VHDL testbenches (VHDL 2008) (with Modelsim)
- Functions, procedures, records, file IO
- Self checking / self stopping
- Coverage

Day 4: Introduction to synthesis (with Synopsys Design Compiler)
- Logic synthesis design flow basics
- Timing constraints
- Optimisation control
- Datapath synthesis
- Clock gate insertion
- Scan insertion

Day 5: Final steps before transferring the netlist to the layout team
- ATPG (with Synopsys TetraMax)
- Power analysis (with Synopsys PrimeTime)
- Formal verification (with Cadence Formality)

EUROPRACTICE
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VHDL language and Design Flow

imec,
Kapeldreef 75, 3001 Leuven,
Belgium

Presented by imec staff

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EUROPRACTICE
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Introduction to Analogue IC Design, Simulation, Layout and Verification
using either a Synopsys Custom Compiler or Cadence Virtuoso flow

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

Presented by STFC staff

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

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Introduction to Analogue IC Design, Simulation, Layout and Verification

This training course introduces the design flow and tools required to successfully analyse and implement modern Analogue IC designs.

The course covers the full flow from schematic entry, through simulation to connectivity-driven layout techniques, sign-off checks and stream out.

The course focuses on best-practice flows for analogue design, simulation and layout, coupled with specific tool knowledge, enabling designers to use a range of analysis techniques and connectivity driven layout on modern CMOS processes. Course attendees will be able to directly apply what they have learnt to their own designs after the course.

Course schedule:

Day 1
- Block-level and system level design flows
- Analogue design infrastructure – technology files and libraries
- Schematic Entry and Editing

Day 2
- Circuit simulation and analyses
- Circuit Parameterisation

Day 3
- Schematic driven layout
- Layout verification – DRC, LVS and Parasitic Extraction
- Post-layout simulation

Theory and concepts are introduced in lectures and practically illustrated in comprehensive lab exercises.

Prerequisites: This course includes introductory material for those unfamiliar with the analogue IC design methodology. All practical exercises will use Linux workstations, so previous experience of using Unix/Linux systems is advantageous.

Advanced Analogue IC Design

This two day course demonstrates advanced simulation practices for analysing sources of variability and explores techniques to mitigate variability through design centring and well matched full custom layout. Tools are introduced for analysing the impact of placement and routing on circuit performance at an early stage in the design flow, informing the creation of implementation constraints which can be used to partially automate the full custom layout.

The aim of this course is to provide attendees with the design flow theory and specific design tool knowledge necessary to design, and implement robust full custom circuits.

This course follows on from our introductory analogue IC courses. Attendees must already have a good working knowledge of the Cadence Virtuoso platform (IC6.1.x), or have attended the either the *'Introduction to Analogue IC Design, Simulation, Layout and Verification'* or *'Introduction to Analogue and Mixed Signal IC Design'* training course first.

Course schedule:
Day 1
- Advanced Analogue Simulation:
  - Corners and Parametric Analysis
  - Sensitivity Analysis
  - Monte Carlo Analysis
  - Circuit Optimisation
  - Yield Optimisation

Day 2
- Advanced Full Custom Layout Analysis:
  - Impact of Layout Dependent Effects (LDE) on device performance and matching
  - Parasitic estimation and partial parasitic extraction flows using Electrically Aware Design (EAD) tools
  - Creating layout using constraints for Constraint-Driven Layout automation
- IO and Floorplanning
  - Chip Finishing

Theory and concepts are introduced in lectures and illustrated in comprehensive hands-on practical exercises using the Cadence Virtuoso suite of tools, with implementation of the design example in the UMC 65nm CMOS process.

This course is aimed at analogue and full custom IC designers who are already familiar with the basic analogue IC design and implementation flow (schematic entry, simulation, connectivity-driven layout, physical verification), but who would like to learn more about advanced tool features to aid robust circuit design.

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Advanced Analogue IC Design
using Cadence tools and a UMC 65nm process

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

Presented by STFC staff

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EUROPRACTICE
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Introduction to Analogue and Mixed Signal IC Design
using a multi-vendor design tool flow and a UMC 65nm process

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

Presented by STFC staff

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

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Introduction to Analogue and Mixed Signal IC Design

This training course introduces the design flows and tools required to successfully analyse and implement analogue dominated mixed signal designs.

The aim of this course is to provide attendees with the design flow theory and specific design tool knowledge necessary to design, simulate and implement analogue-centric mixed signal designs in modern CMOS processes.

The first half of the course studies a basic analogue block level design flow from schematic entry, through simulation, to connectivity-driven layout techniques, sign-off checks and stream out. The second half of the course examines how the analogue design flow can be extended to implement mixed signal designs dominated by analogue blocks (i.e. Big A design).

Course schedule:

Day 1
- Block-level and system level design flows
- Analogue design infrastructure – technology files and libraries
- Schematic Entry and Editing

Day 2
- Circuit simulation and analyses
- Specification-driven simulation
- Schematic driven layout

Day 3
- Post-layout simulation
- Layout verification – DRC, LVS and Parasitic Extraction

Day 4
- Big A design flow and simulation strategies
- Simulation speed and accuracy trade-offs when modelling at different levels of abstraction
- Design considerations and physical constraints at interfaces between digital and analogue blocks

Day 5
- Physical implementation and chip assembly
- Interaction and data transfer between full custom and digital design platforms

Theory and concepts are introduced in lectures and illustrated in comprehensive hands-on practical exercises utilising the Cadence Virtuoso suite, other supporting tools from the EUROPRACTICE portfolio, and implementation of the design example within the UMC 65nm CMOS process.

Prerequisites: Circuit design theory is outside the scope of this course so knowledge of basic circuits is required. All practical exercises will use Linux workstations, so previous experience of using Unix/Linux systems is advantageous

Digital Mixed Signal design and implementation

This training course is aimed at designers already familiar with a basic IC implementation flow who wish to go further to integrate and use full custom/analogue blocks within a larger digital system.

Theory, concepts and trade-offs influencing design decisions for a digital-centric 'Big Digital' mixed signal design flow are introduced in lectures and illustrated in comprehensive hands-on practical sessions using a multi-vendor flow with design tools from Cadence, Mentor and Synopsys.

The aim of this course is to provide attendees with the theory and specific tool knowledge necessary to design, simulate and implement their digital-centric mixed signal designs in modern CMOS processes, enabling attendees to directly apply the skills acquired to their own projects after the course.

Course schedule:

Day 1
- Trade-offs between simulation speed and accuracy when modelling at different levels of abstraction
- Design considerations and physical constraints at the interface between digital and analogue blocks

Day 2
- Interaction and data transfer between analogue-centric and digital-centric tools
- Analogue block characterisation: timing and layout abstract generation
- Integration of analogue IP into a digital system

Day 3:
- RTL synthesis with analogue macros
- Physical implementation and chip finishing

Prerequisites: The focus of this course is on the theory behind the digital-centric mixed signal design flows. This course is not intended to provide exhaustive training in the use of the tools and assumes that attendees have experience and knowledge of basic IC design and implementation tools and flows.

Attendees who do not have this prerequisite knowledge are advised to first attend our introductory courses on digital and analogue IC design which provide a solid grounding in the basic design flow and tools.

Attendees may find that some familiarity with Verilog and Verilog-AMS would be beneficial, but is not essential. All lab exercises are run on Linux workstations, so previous experience of using UNIX/Linux systems is helpful.

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Digital Mixed Signal design and implementation
using a multi-vendor design tool flow and a UMC 65nm process

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

Presented by STFC staff

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

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EUROPRACTICE
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Verilog and SystemVerilog for Digital Design

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

Presented by STFC staff

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Verilog and SystemVerilog for Digital Design

This course provides delegates with a broad introduction to Verilog and SystemVerilog for the design of digital circuits and systems.

This course starts by covering the core Verilog language features. It then progresses to examining coding for synthesis before moving on to FSM design and parameterization. SystemVerilog language constructs for design are also explored. This course is suitable for both beginners and existing VHDL designers who want to adopt Verilog and SystemVerilog for design.
By the end of the course, attendees should be able to:

- Efficiently develop Verilog and SystemVerilog RTL designs, and simulate them to verify their functionality
- Write self-checking testbenches
- Check designs with lint tools
- Synthesize designs and check the timing results
- Perform gate level simulation

Course schedule:

Day 1
- Introduction to Verilog and simulator fundamentals
- Verilog basics, design hierarchy and simulation
- Continuous and procedural assignments

Day 2
- Data types, operators and arithmetic
- Testbenches and testbench constructs
- File IO, subroutines, and response checking
- Simulation debug
- Introduction to synthesis
- Coding synthesisable RTL design

Day 3
- Linting and RTL signoff
- Parameterized design
- Finite State Machine (FSM) coding

Day 4
- Gate-level simulation
- SystemVerilog design constructs
- SystemVerilog data types

The extensive practical hands-on sessions give delegates the chance to use a variety of tools from the EUROPRACTICE Design Tool portfolio:

- Simulators: Cadence Incisive, Mentor Questa, Synopsys VCS-MX, or Xilinx Vivado
- Synthesis tools: Cadence Genus, Cadence RTL Compiler, Synopsys Design Compiler, Synopsys Synplify, Mentor Precision, Altera Quartus or Xilinx Vivado
- Linting tools: Cadence Incisive HAL or Synopsys SpyGlass

Prerequisites: A basic understanding of digital circuits and sequential elements is required.

Verification for Digital Designs

This course introduces modern functional verification techniques to intelligently and efficiently verify digital designs.

The aim of this course is to enable attendees to improve the quality of their digital design by application of modern verification techniques including coverage-driven verification, assertion-based verification, and formal and static verification. The concepts presented in lectures are accompanied with guided hands-on practical exercises which demonstrate the techniques and the appropriate use of design tools.

By the end of the course, attendees should be able to:

- Plan and measure verification closure
- Understand the strengths and weaknesses of different verification techniques
- Create self-checking testbenches
- Create UVM testbenches
- Create assertions for both simulation and formal proof
- Apply linting for regression checking and RTL signoff
- Apply CDC checks on multi-clock designs

Course schedule:

Day 1: Introduction and coverage-driven verification
- Overview of functional verification
- Verification planning and management
- Testbench design and debugging
- Using untimed (C/C++/SysC) reference models in testbenches
- Regression suites

Day 2: SystemVerilog for Verification
- Constrained-random verification and transaction-level modelling using SystemVerilog classes
- Universal Verification Methodology (UVM)
- Assertion-based verification and SystemVerilog assertions

Day 3: Static and formal design verification
- Formal property checking
- Linting and RTL signoff
- Clock-domain crossing verification for multi-clock designs

The course is suitable for designers using VHDL, Verilog or SystemVerilog, and whilst SystemVerilog is used for the more advanced testbenches and assertions, these SystemVerilog concepts are fully explained. The hands-on practical exercises will use Cadence tools.

Prerequisites: General knowledge of digital design and basic knowledge of VHDL or Verilog/SystemVerilog is required. Familiarity with UNIX environment would be helpful but is not essential.

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Verification for Digital Designs
illustrated with Cadence tools for the practical sessions

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

Presented by STFC staff

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EUROPRACTICE
TRAINING COURSES

Introduction to STMicroelectronics Technologies
multiple courses on different specific technologies offered

CMP,
6, Avenue Félix Viallet, 38031 Grenoble, France

Presented by CMP and STMicroelectronics staff

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

Only pre-booked and confirmed delegates may attend. Attendance is also subject to payment of course fees and signature of appropriate technology non-disclosure agreements and tool license agreements.

For further details, course dates and online booking:

www.europractice.stfc.ac.uk

Introduction to STMicroelectronics Technologies

STMicroelectronics and CMP organise a series of two-day training courses on various technologies from STMicroelectronics

STMicroelectronics 28nm FDSOI technology.

This course gives an overview of the major analogue, digital and RF features of the STMicroelectronics 28nm FDSOI technology. The benefits of FD-SOI technology are described including how to take full advantage of wide voltage range body biasing optimisation.

Various categories of circuits (digital, analog/RF and mmW) are explored and the main design features specific to FD-SOI and the expected performance are examined. Simulation, verification and demos conclude the training.

Course schedule:

Day 1
- Technology overview
- Analog/RF circuits: benefits of FD-SOI Technology
- Technology process features, layers and metal stack options
- 28FDSOI strategy offer
- Design Kit structure and content

Day 2
- Front end simulation, model & corner use
- Back end flow: Physical verification (DRC, LVS)
- Back end flow: Parasitic Extraction (PEX) and Post layout simulation (PLS)
- Demos.

STMicroelectronics 55nmBiCMOS technology:

This course gives an overview of the major analogue, mixed-signal and RF features of STMicroelectronics 55nm BiCMOS technology.

Then follows a focus on the benefits of 55 BiCMOS technology, to address demanding optical, wireless and high-performance analog applications. Various categories of circuits (digital, analog/RF and mmW) are explored and the main design features specific to BiCMOS55 and the expected performance are examined. Simulation, verification and demos conclude the training.

Introduction to GLOBALFOUNDRIES 22nm FDSOI Technology

An in-depth technical Seminar introduction to GLOBALFOUNDRIES 22nm FDSOI technology presented by staff from GLOBALFOUNDRIES.

The aim of this two-day technical seminar is to enable designers of high performance integrated circuits to understand the design methodology for the complex and advanced FDSOI technology of GLOBALFOUNDRIES.

- 22nm FDSOI introduction
- Analog and Mixed “Best practices”
- Reference flows
- Technology information and MPW submission for all GLOBALFOUNDRIES technologies

Technical Seminar schedule:

Day 1
- Introduction to GLOBALFOUNDRIES and general overview of 22nm FDSOI technology
- Analog and Mixed Signal “Best Practices”
- Regular well and Flipped-well NFET/PFET body biasing
- Mismatch and corner simulations

Day 2
- Digital design flow and Synthesis with Cadence
- Layout constraints and Signoff
- RF components
- MPW participation procedure through Europractice
- Q&A wrap up

Please note that this event is an in-depth technical seminar and does not include hands-on practical sessions.

Prerequisites: Seminar participants should be familiar with circuit and IC design.

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Introduction to GLOBALFOUNDRIES 22nm FDSOI Technology

Fraunhofer IIS,
Am Wolfsmantel 33, 91058 Erlangen, Germany

Presented by Fraunhofer in partnership with staff from GLOBALFOUNDRIES

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

Only pre-booked and confirmed delegates may attend. Attendance is also subject to payment of course fees and signature of appropriate technology non-disclosure agreements and tool license agreements.

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EUROPRACTICE
TRAINING COURSES

Hardware Security

imec,
Kapeldreef 75, 3001 Leuven,
Belgium

Presented by imec in partnership with staff from KU Leuven

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Hardware Security

This course focuses on digital IC and system design techniques that are needed to design secure ICs and systems in different application domains. Our hands-on learning approach enables the participant to directly apply the learned content in to their projects.

Security and privacy are essential to execute everyday electronic activities. It is used in a wide range of applications such as electronic payments, communications, identity cards, e-voting, smart homes, e-health, automotive, internet of things, cloud computing and many more. This requires efficient and secure implementations of cryptographic algorithms and protocols both in embedded context as well as on high end processors and servers.

Implementations of these algorithms and protocols need to be efficient, in terms of area or energy consumption when included in a portable embedded device, or provide high throughput, e.g. for high speed interconnects. This course will introduce the topic.

Course Objectives

- To learn about the state-of-the-art of security, encryption and security threats
- To learn about the hard- and software co-design for security and cryptography
- To learn about secure implementations resistant to passive and active attacks
- To learn about the security building blocks like random number generators and physically unclonable functions

Course schedule:

Part I: Introduction to security and privacy
- state of the art and threat models

Part II: HW/SW co-design for security and cryptography
- Implementations of secret key algorithms: DES, 3DES, AES, light-weight algorithms
- Implementation aspects of public key algorithms

Part III: Secure implementations resistant to passive and active attacks
- Analysis of electronic attacks on implementations
- Passive side-channel attacks and active fault attacks
- Design and cost evaluation of countermeasures

Part IV: hardware security building blocks:
- Random number generation and testing
- Physically unclonable functions
- Design methods for security

Prerequisites: Basic knowledge of digital hardware and embedded system design for ASIC, FPGA and/or embedded micro-controllers.

Essential verification with SystemVerilog and UVM

This course gives an in-depth introduction to the advanced verification methodologies through extensive features of SystemVerilog and Universal Verification Methodology (UVM). This course further discusses the benefits of the SystemVerilog constructs and features, verification efficiency and productivity gain through this methodology. SystemVerilog verification features include abstract classes, constrained random stimulus, coverage, assertions, queues and dynamic arrays for an effective and efficient verification.

This five-day course covers all the necessary basics of SystemVerilog for verification, Assertions and UVM. After this course, the enlightened audience should be able to create their own verification scenario, self-learn the advanced concepts and methodology of UVM and also to implement it in an effective and reusable way.

Day 1: SystemVerilog for verification
- Verification overview and present/future requirements
- Introduction to SystemVerilog for verification environments
- Data types, operators and literals
- Procedural and control statements

Day 2: SystemVerilog for verification
- Subroutines and Interfaces
- Arrays (dynamic and associative arrays) and queues
- Object oriented design/verification
- TLM level modeling

Day 3: SystemVerilog for verification
- Random stimulus and randomization
- Class and virtual class randomization
- Coverage and cover group
- Other advanced verification techniques
- CPF/UPF for power island simulation
- Coding rule checkers

Day 4: Assertion based verification
- Introduction to assertions
- SV-assertions and SVA checker library
- Assertions, property checkers, sequences
- Basic and advanced SVA constructs
- Assertion coverage, how much coverage is enough
- Introduction to OVL and using OVL along with SVA

Day 5: UVM: Universal verification methodology
- What should a ‘verification environment’ look like?
- Big vs. small projects
- What is UVM? How to use UVM?
- Component level test benches at top-level (passive agents)
- Power of assertions in UVM
- The power of sequences and sequencers

Prerequisites for this course are being familiar with VHDL, Verilog, or C++. The minimum prerequisites opens the door to a large audience to enhance their understanding of System to RTL level verification.

EUROPRACTICE
TRAINING COURSES

Essential verification with System Verilog and UVM

imec,
Kapeldreef 75, 3001 Leuven,
Belgium

Presented by imec staff

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

Only pre-booked and confirmed delegates may attend. Attendance is also subject to payment of course fees and signature of appropriate technology non-disclosure agreements and tool license agreements.

For further details, course dates and online booking:

www.europractice.stfc.ac.uk

EUROPRACTICE
TRAINING COURSES

Photonic Integrated Circuits (PIC)

The use of CMOS fabrication technology has enabled large scale integration of photonic components at chip level – called Photonic Integrated Circuits (PICs). The concepts of fabless manufacturing and multi-project-wafer (MPW) services are now widely available for PICs, for various base materials. Low-cost access to generic fabrication processes for rapid prototyping and low volume production has shifted the emphasis to design innovation.

This course intends to introduce basics of PIC technology and provide introductory hands-on training on PIC design. The training is structured in two parts:

- The first part is seminar-based and focuses on the basics of PIC technology through seminars delivered by experts from the PIC industry and academia.
- The second part running over two days, focuses on PIC design through hands-on training.

The training is divided into two parts: seminars (1 day) and hands-on sessions (2 days). Participants, depending on their requirements, can attend either Part 1 (Technology Overview), Part 2 (Design Overview), or both.

Course outline:

Day 1: PIC Technology Overview
- Europractice & Photonics MPW services (imec & STFC)
- Presentations by the leading European PIC foundries on of the state-of-the-art of their PIC platforms (Silicon photonics, Silicon Nitride photonics, packaging etc.)
- Presentations on PIC design flows and challenges by design experts.

Day 2 and Day 3: PIC Design Tutorial
- Extensive hands-on practical sessions with photonics design automation tools, including use of design kits and addressing PIC design challenges
- Practical Tour (Cleanroom Tour / Lab Tour)
- Hands-on: Build your own design under guidance

Minimal prerequisites for this course open the door to a wide audience, including managers, to enhance their understanding of silicon photonics.

Photonic Integrated Circuits (PIC)

imec,
Kapeldreef 75, 3001 Leuven,
Belgium

Presented by imec staff and invited speakers

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

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Tutorial on IHP SG25H4EPIC Technology for Electronic-Photonic ICs

An intensive course on electronic-photonic IC (EPIC) design methodology using the IHP design kit

The aim of this course is to enable designers of high performance integrated circuits to understand the design methodology for electronic-photonic ICs and gain insight into the design flow implemented for the IHP SG25H4EPIC technology.

The practical examples given are based on 0.25 µm SiGe:C photonic BiCMOS technology and Cadence 6.1.5, design steps will be practised on workstations. Course contents:

- Electronic-photonic design kit (overview & installation)
- Schematic & layout of a simple EPIC design
- Technology information and MPW tape-in procedure

Course program:

Day 1 IHP Mixed signal flow
- Opening remarks
- Electronic-photonic design kit (overview, installation, hands-on)
- Design kit documentation
- Parametric layout of an optical DBPSK receiver with IPKISS (Notebook on layout generation with Python scripts in IPKISS)
- Simple EPIC design example from schematic to layout (hands-on)

Day 2 IHP Mixed signal flow
- MPW service and tape-in procedure
- Usage of an existing 25 Gbps TIA design IP (on abstract level) in an EPIC design flow (hands-on)
- Design kit support

Prerequisites: Course participants should be familiar with circuit design. Familiarity with Cadence design tools would be helpful.

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EUROPRACTICE
TRAINING COURSES

Tutorial on IHP SG25H4EPIC Technology for Electronic-Photonic ICs

Fraunhofer IIS,
Am Wolfsmantel 33, 91058 Erlangen,
Germany

Presented by Fraunhofer in partnership with staff from IHP

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

Only pre-booked and confirmed delegates may attend. Attendance is also subject to payment of course fees and signature of appropriate technology non-disclosure agreements and tool license agreements.

For further details, course dates and online booking:

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EUROPRACTICE
TRAINING COURSES

Photonic component, circuit and systems design using Lumerical Tools

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

Presented by STFC in partnership with staff from Lumerical

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

Only pre-booked and confirmed delegates may attend. Attendance is also subject to payment of course fees and signature of appropriate technology non-disclosure agreements and tool license agreements.

For further details, course dates and online booking:

www.europractice.stfc.ac.uk

Photonic component, circuit and systems design using Lumerical Tools

Learn how to apply Lumerical's suite of products to address the challenges of photonic component, circuit, and systems design. Attendees will obtain instruction in the main product features of FDTD Solutions, MODE Solutions, DEVICE and INTERCONNECT, applied across a wide variety of applications.

The course will begin with an overview of the main features of the Lumerical tool suite, before focusing in greater detail on the use of the individual products. Practical sessions, where attendees work through hands-on examples, putting into practice the principles outlined in lectures, are a key component of each section.

- **FDTD Solutions** 3D FDTD propagation solver for the simulation and optimization of photonic devices and structures. In this session users will cover the optimal use the major product features. Practical session examples include:
  - Particle scattering
  - Plasmonic metamaterials
  - Waveguide couplers

- **MODE Solutions** versatile mode solver and propagation simulator for the design, analysis and optimization of waveguide structures, components and subsystems. Practical session examples include:
  - Waveguides
  - Optimizing edge couplers

- **DEVICE.** DEVICE includes powerful 2D and 3D charge transport (CT), heat transport (HT) and optical (DGTD) solvers. It is specifically designed to operate with FDTD Solutions and MODE Solutions to solve optoelectronic structures such as solar cells, CMOS image sensors, modulators and high speed photodiodes. Practical session examples include:
  - Electro-optical modulator

- **INTERCONNECT** photonic integrated circuit (PIC) design environment, for the analysis of integrated optical circuits, silicon photonics components, and optical interconnects. Practical session examples include:
  - Mach-Zehnder modulators for transceiver applications
  - Mach-Zehnder optical bio-sensing circuit

Finally, the course will conclude with a Question & Answer session, giving attendees an opportunity to discuss their research, and receive feedback on best-practice approaches for applying the Lumerical tools.

Prerequisites: The course will span introductory training using the Lumerical products through to advanced topics. The event is suitable for all levels, although a basic familiarity with the Lumerical tools would be helpful and can be gained by watching the product introductory webinars prior to attending.

Introduction to Technology CAD (TCAD)
using Synopsys Sentaurus Tools

This training course provides instruction in the use of the Synopsys Sentaurus TCAD tool suite for the simulation of semiconductor devices.

Working through a combination of lectures and hands-on practical exercises, attendees will learn how to apply predictive semiconductor fabrication process modelling, and the means to establish and optimise the electrical behaviour of a broad range of semiconductor devices -- including nano-scale CMOS structures, optoelectronic devices, and radiation detectors --through simulation.

The course will cover the following main topics:

- Creating and managing parameterised TCAD simulation projects using the Sentaurus Workbench framework package
- Simulating semiconductor device fabrication using Sentaurus Process
- Using Sentaurus Structure Editor to create device structures
- Undertaking device simulations to determine a structure's electrical behaviour using Sentaurus Device
- The application of the Sentaurus Electromagnetic Wave Solver to simulate optoelectronic devices
- The conversion and manipulation of simulation results using Sentaurus Data Explorer

The course is suitable for microelectronic engineers who are new to TCAD, and are interested in applying semiconductor device simulation in their work. Prior understanding of basic semiconductor device physics would be helpful.

Course schedule:

Day 1
- Overview of TCAD and the Synopsys Sentaurus TCAD Tools
- Introduction to the Sentaurus Workbench
- Visualisation of Sentaurus TCAD results
- Introduction to process simulation and Sentaurus Process
- Creating radiation detector device process simulation using Sentaurus Process

Day 2
- Introduction to Sentaurus Structure Editor
- Creating FD-SOI device structure using Sentaurus Structure Editor
- Introduction to device simulation and Sentaurus Device

Day 3
- Introduction to Sentaurus Electromagnetic Wave Solver
- Undertaking an example optical semiconductor device simulation of a solar cell structure
- Introduction to Sentaurus Data Explorer

EUROPRACTICE
TRAINING COURSES

Introduction to Technology CAD (TCAD)
using Synopsys Sentaurus Tools

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

Presented by STFC staff

This training course will accept bookings from Professors, Lecturers, Academic Staff and postgraduate students from established academic sites who are Members of EUROPRACTICE.

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EUROPRACTICE
TRAINING COURSES

Introduction to MEMS – IC co-design

using Coventor MEMS+ and Cadence Virtuoso

A short course introducing MEMS-IC co-design using Coventor MEMS+ coupled to Cadence Virtuoso. Aimed at IC designers who wish to gain an insight into the design flow necessary to incorporate a MEMS device in their work.

This course exploits the integration of the MEMS design package Coventor MEMS+ 6 with the Cadence Virtuoso IC design tools, covering: design entry, layout synthesis, electro-mechanical component simulation, MEMS/ IC co-simulation, and physical verification by automated DRC.

Participants will be provided with a high-level overview of MEMS technology and an outline of best-practice approaches to creating a device using component building blocks.

Extensive hands-on practical sessions will follow the design and analysis of an accelerometer using the SOIMUMPS MEMS fabrication process. This will include the generation of the model for inclusion in Cadence Virtuoso for simulation with a behavioural IC circuit.

The transient response of the reference MEMS device will be determined while embedded in a sigma-delta force feedback loop - a situation unfeasible to analyse using the conventional FEA approach to MEMS simulation.

The procedure for the automatic layout generation will be demonstrated, and a basic DRC check will be performed to complete the MEMS design flow.

Course schedule:

Day 1

- Creating a MEMS process description for MEMS+
- MEMS design entry
- MEMS characterisation: Transient, AC, and Pull-in analysis

Day 2

- Advanced simulation techniques: PSS and Noise analysis
- MEMS and IC co-simulation with closed-loop force-feedback
- Design Rule Checking (DRC)

Prerequisites: No previous knowledge of MEMS or IC design is necessary. The course will not cover the full use of IC design software (This is covered in the Introduction to Analogue and Mixed Signal IC Design course.) Previous experience of using UNIX/Linux systems is advantageous.

Introduction to MEMS – IC co-design
using Coventor MEMS+ and Cadence Virtuoso

STFC Rutherford Appleton Laboratory,
Didcot, Oxfordshire, OX11 0QX
UK

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For further details, course dates and online booking:

www.europractice.stfc.ac.uk

Training Courses

Circuits Multi-Projet®/CNRS-Grenoble-INP-UGA
Grenoble, France

Fraunhofer-Institut für Integrierte Schaltungen IIS
Erlangen, Germany

Interuniversitair Micro-Electronica Centrum
Leuven, Belgium

Science and Technology Facilities Council
Rutherford Appleton Laboratory, Didcot, UK

Tyndall National Institute
University College Cork, Ireland

www.europractice.com